# Implementation of a Triple-Mode SDR Handset Modem

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## ABSTRACT

In this paper, we present a Software Defined Radio (SDR) handset modem which supports cdma2000, Time Division Duplex High-Speed Downlink Packet Access (TDD HSDPA), and Wireless Broadband Portable Internet (WiBro). The proposed modem employs digital signal processors (DSPs), field programmable gate arrays (FPGAs), and microprocessors, so that the various communication functions of cdma2000, HSDPA and WiBro can be programmed by software downloaded onto the hardware platform. The proposed handset modem comprises several blocks that are interfaced through protocols such as low voltage differential signaling (LVDS), external memory interface (EMIF), and multi-channel buffered serial port (McBSP). The proposed SDR handset modem is used for the physical layer of the mobile communication system network. We first describe the structure of the cdma2000, HSDPA, and WiBro systems. Then, the mapping of the modem functions onto the available processing resources is detailed for each SDR mode. Finally, the performance of the proposed SDR handset modem is demonstrated based on internal loopback tests with the test vectors.

## 1. INTRODUCTION

An SDR system is a new form of radio communication system which supports various communications just by downloading new software. It is a reconfigurable system which can be applied to a variety of wireless communication systems. In this paper, we address the implementation of a triple-mode SDR handset modem developed using the TI TMS320C6416T and TMS320C6713 DSPs, and FPGAs. A triple-mode SDR handset modem can certainly improve flexibility and efficiency. We focus on a triple-mode SDR handset with HSDPA, WiBro, and cdma2000 capabilities.

In this paper we first describe the HSDPA, WiBro, and cdma2000 systems. Then, we propose the implementation and the functional allocation of each hardware module. Finally, we demonstrate the performance of our hardware through experimental results.

## 2. SYSTEM AND IMPLEMENTATION

### 2.1 TDD HSDPA, WiBro, and cdma2000

*2.1.1 TDD HSDPA system*

HSDPA technology, which appends access technique for high speed downlink transmission, is the evolution of existing asynchronous IMT-2000. In HSDPA data can be downloaded at maximum speed of 14 Mbps, i.e., seven times faster than WCDMA (Release 4). HSDPA supporting both FDD mode and TDD mode is designed to coexist with WCDMA by using the same channelization code resource as existing FDD mode (which uses 3.84 Mcps chip rate within 5 MHz band) or the broadband TDD mode system. Also narrowband TDD mode HSDPA is designed to coexist with other narrowband systems using 1.28 Mcps. HSDPA is considered an advancement of WCDMA (WCDMA Release 5 specifies HSDPA). Thus, 3.5G systems benefit from higher of transmission speed, frequency reuse efficiency, and lower cost. Fig. 1 shows the block diagram of terminal transmitter and base station receiver in HSDPA system.

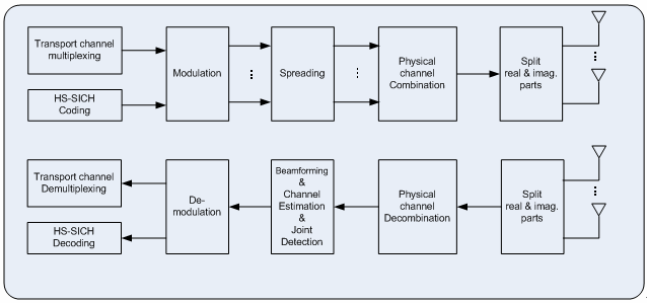


Fig. 1: Block diagram of HSDPA system

The base-station receiver comprises 1) the splitter, which outputs the real and imaginary part of the received signal, 2) the physical channel decombinator, which divides the transmitter signal using individual Orthogonal Variable Spreading Factor (OVSF) for each user, 3) the beamforming block, which optimizes the beampattern, 4) the channel estimation block, which compensates for the data distortion due to channel fading, 5) the demodulator, which demodulates the received signal, and 6) the decoding block,

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which decodes high speed shared information channel (HS-SICH) that performs adaptive modulation and coding (AMC) [1-4].

*2.1.2 WiBro system*

WiBro is an OFDM-based, portable data communication service that operates in the 2.3 GHz frequency band, providing data rates of up to 20 Mbps over distances of up to 1 km for terminal speeds that can exceed 60 km/h. Note that WiBro provides service coverage over a radius ten times larger than that of the wireless LAN system also known as Wi-Fi (which only provides hot-spot service area coverage). The WiBro high-speed portable internet (HPI) standard, mainly developed in Korea, corresponds to the IEEE 802.16e international technical standard, which was recently adopted for next generation wireless broadband systems.

In WiBro frame duration is 5 ms. A frame starts with the preamble, followed by downlink (DL), transmit transition gap (TTG), uplink (UL), and receive transition gap (RTG). The concept is shown in Fig. 2. The DL supports 27 symbols and 30 subchannels, and consists of preamble, frame control header (FCH) with DL_MAP information, DL_MAP, and two-dimensional DL_Bursts. The UL supports 15 symbols and 35 subchannels, and consists of 1 dimension UL_Burst and Ranging subchannel. The DL and UL have their own basic structure. For DL, the basic structure is a cluster. A slot, which is the minimum unit, is made of two clusters. For UL, the basic structure is a tile. A slot is constructed from 6 tiles.

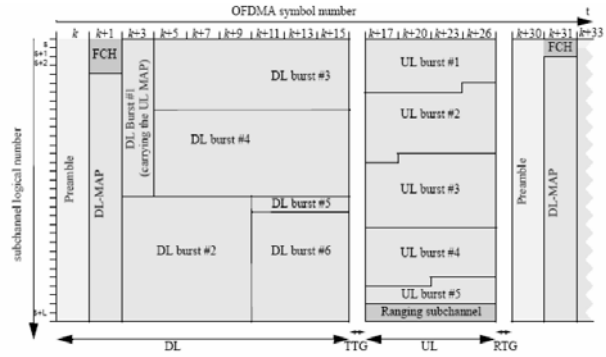


Fig. 2: Structure of WiBro frame

WiBro data transmission procedures include symbol processing, modulation, pilot subcarrier insertion, IFFT, and permutation. Symbol processing consists of randomization, encoding, and interleaving for each data block. Pilot subcarrier insertion adjusts the data to the WiBro frame structure. The reception procedure is practically the reversal of the transmission procedure. The system block diagram is shown in Fig. 3 [5].

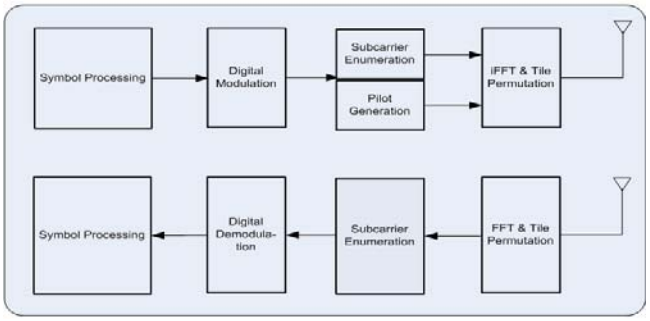


Fig. 3: Block diagram of WiBro system

*2.1.3 The cdma2000 system*

The cdma2000 system is a specification for Direct-Sequence Code Division Multiple Access (DS/CDMA) system, where 1.25 MHz bandwidth and 1.2288 Mcps spreading code are used to transmit signals. The cdma2000 frame structure is specified in [6]. Fig. 4 shows the block diagram of our cdma2000 modem implementation. This modem supports cdma2000 forward link functions related to processing pilot and fundamental channels. Each base station broadcasts its own pilot signal in its coverage area. The pilot is used to find the multipath delay timing, referred as "searching", and to estimate the phase distortion due to channel propagation. The "fingers" comprise despreading and channel phase distortion estimation, and are assigned to each resolvable multipath. After combining the finger outputs (rake receiver) the signal is sent for deinterleaving, depuncturing, and decoding.

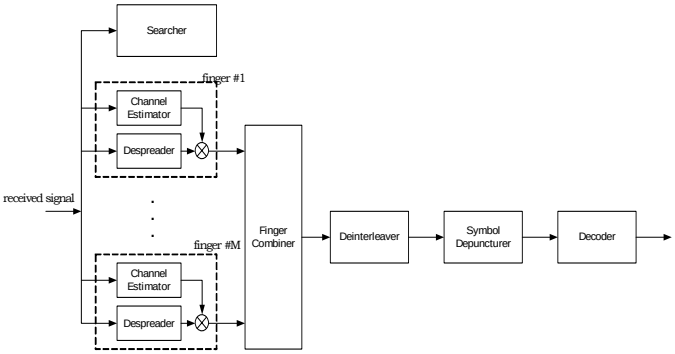


Fig. 4: Block diagram of cdma2000 receiver

**2.2 System Implementation**

*2.2.1 Implementation of modem hardware*

Fig. 5 shows that the triple-mode SDR handset modem consists of one TMS320C6416T, one TMS320C6713, two FPGAs, one DPRAM, and one MPC8260 module. The FPGAs are connected by several kinds of interfaces such as five channels of differential pair, 32-bits general purpose input/output, and differential pair using dedicated LVDS

chip, DS92LV18. The two DSPs are connected to the FPGA #2 by EMIF and use McBSP for communicating with each other. Each DSP has SDRAM and FLASH memory connected by EMIF. For signal flow efficiency we used Sync DPRAM (IDT70V3319) with FPGA #2. The MPC8260 Module interface is connected to the FPGA #1 by 60xBUS and to the two DSPs by HPI.

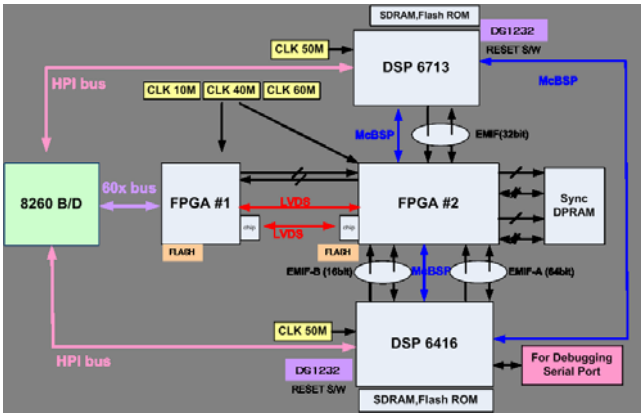


Fig. 5: Block Diagram of triple-mode SDR handset modem

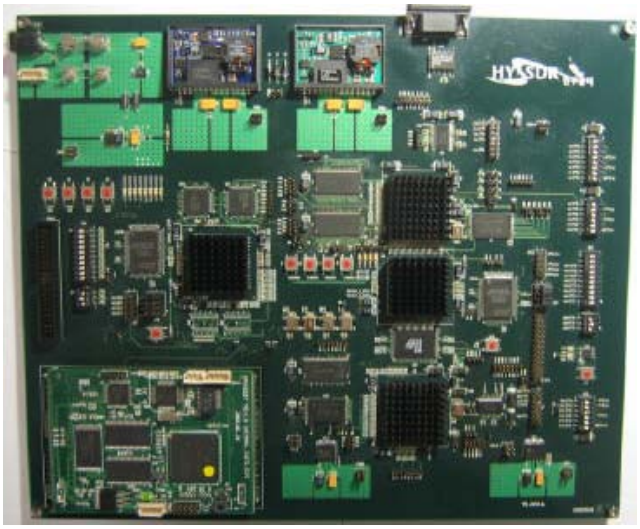

Fig. 6: Photograph of the triple-mode SDR handset modem

The 5V input voltage from the external source (such as power supply) changes into 3.3V, 2.5V, 1.4V, and 1.2V through DC-DC converter: 3.3V is commonly supplied voltage for a wide range of devices, 1.4V for TMS320C6713, 1.2V for TMS320C6416T, 2.5V and 1.2V for FPGAs. The two DSPs have basic clock of 50 MHz and the two FPGAs have clocks of 10, 40, 50, and 60 MHz. Fig. 6 is a photograph of the triple-mode SDR handset modem.

*2.2.2 Implementation of TDD HSDPA modem*

There are two DSP modules in the triple-mode SDR handset mode. Their communication mode is reconfigurable through software download. Different functions can be allocated to each DSP by the downloaded mode.

Fig. 7 shows a block diagram of HSDPA functions. Received data is generated in FPGA #1 and sent to FPGA #2 through the LVDS interface. FPGA #2 transfers it to the TMS320C6713 DSP for channel estimation and joint detection process. The result passes through FPGA #2 and on to the TMS320C6416T DSP for demodulation and Viterbi decoding. Output data is sent to TMS320C6713 for monitoring , i.e., checking BER/FER.

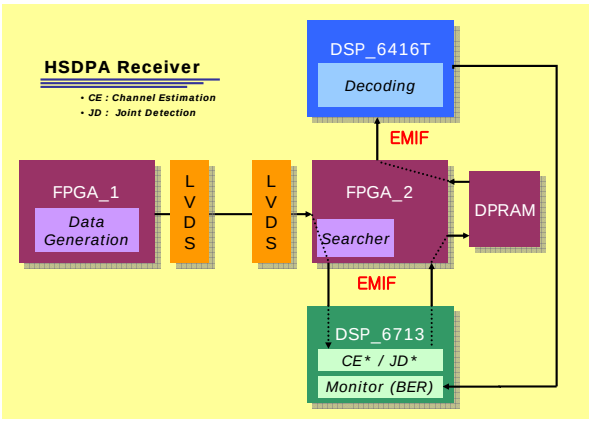


Fig. 7: Function assignment for HSDPA mode

*2.2.3 Implementation of WiBro modem*

Fig. 8 illustrates a block diagram of transmitter and receiver in WiBro uplink. In transmitter, data which go through channel coding is generated. This coded data is allocated to uplink frame with pilot, and re-allocated by tile and subcarrier following a permutation formula. After IFFT and cyclic prefix (CP) addition the signal is transmitted. The receiver combines data from each path, performs synchronization and CP removal, followed by FFT, tile depermutation, channel effect compensation, subcarrier depermutation, digital demodulation, and channel decoding [7].

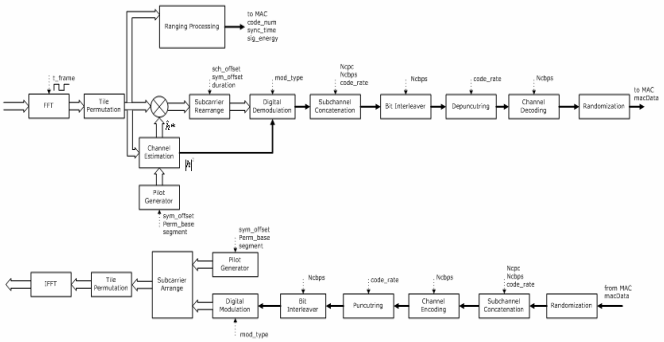

Fig. 8: Block diagram of WiBro uplink

Fig. 9 shows a block diagram of WiBro functions. WiBro data is generated in FPGA #1 and sent to FPGA #2 by LVDS interface. FPGA #2 removes CP and passes the signal on to the TMS320C6416T for channel estimation, FFT, Viterbi decoding and demodulation process. The processed data passes through FPGA #2 with DPRAM and then on to TMS320C6713 for monitoring. Then we can check BER and FER.

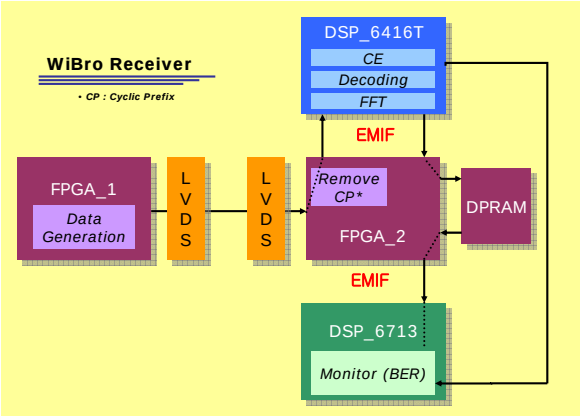


Fig. 9: Function assignment for WiBro mode

*2.2.4 Implementation of cdma2000 modem*

Fig. 10 illustrates the assignment of functions to each programmable device to support the cdma2000 mode. FPGA_2 implements the function of searching the multipath timing. TMS320C6416T implements despreading, channel estimation, symbol processing, and decoding functions. The decoding results are gathered and stored in TMS320C6713 to monitor the performances.

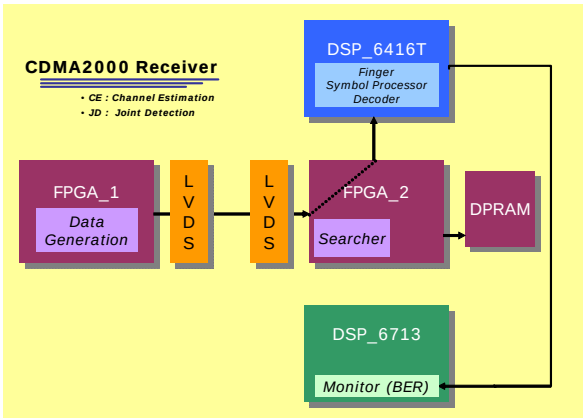


Fig. 10: Function Assignment for cdma2000 mode

## 3. PERFORMANCE ANALYSIS

This section presents numerical performance results for the SDR handset modem operating in WiBro, HSDPA and cdma2000 modes. Transmitted data which experiences communication channel imperfections is computer-simulated. Received data is passed through the FPGAs and DSPs for processing, as shown in Fig. 11.

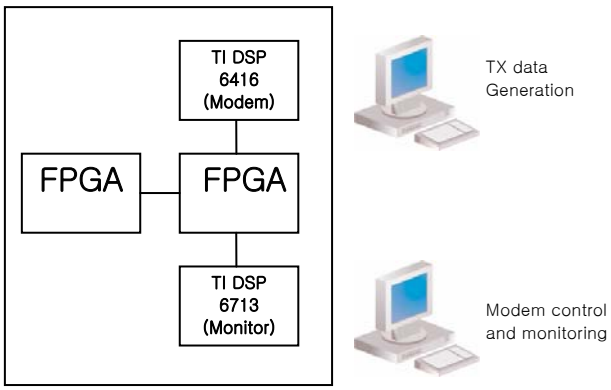


Fig. 11: Configuration of triple-mode SDR handset modem performance test

### 3.1. TDD HSDPA Modem Performance Analysis

*3.1.1 AWGN*

Fig. 12 illustrates the uncoded bit-error-rate (BER) performance in AWGN environment from implemented board using QPSK modulation. Note that the BER performance for the single-user case is as same as that of multiple users transmitting data simultaneously. As well, it is observed that the BER performance is $10^{-3}$ at about 6.8 dB.

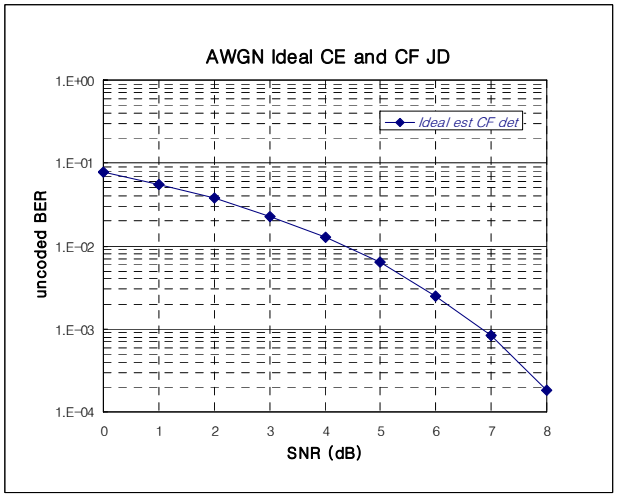


Fig. 12: Uncoded BER performance in AWGN channel

*3.1.2 Rayleigh fading*

Fig. 13 illustrates the uncoded bit-error-rate (BER) performance in Rayleigh fading environment (1-path), for QPSK modulation. As shown in the figure the BER performance is varies slightly with the number of users. As well, it is observed that the BER performance is $10^{-3}$ at about 25 dB.

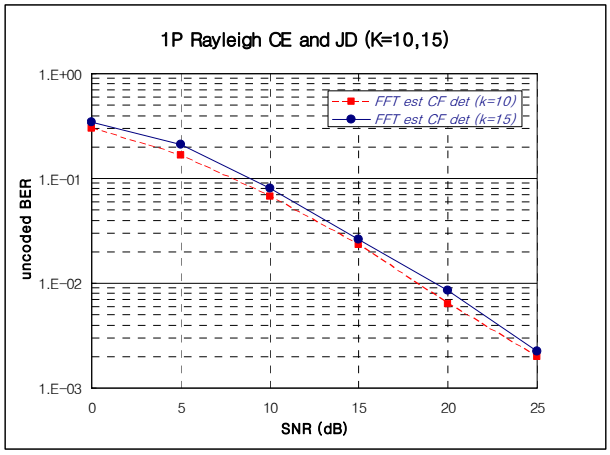


Fig. 13: Uncoded BER performance in Rayleigh channel

### 3.2 WiBro Modem Performance Analysis

*3.2.1 AWGN*

Fig. 14 illustrates uncoded and coded BER performance in AWGN environment with QPSK modulation scheme. Note that the coding gain is about 5 dB at the BER $10^{-2}$ [8].

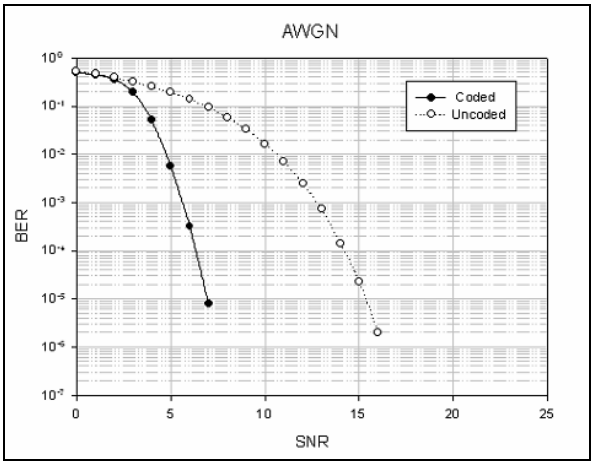


Fig. 14: BER Performance in AWGN channel

*3.2.2 Rayleigh fading*

Fig. 15 illustrates uncoded and coded BER performance in Rayleigh fading environment, for QPSK. Note that the coding gain is about 5 dB at the BER $10^{-2}$ [9].

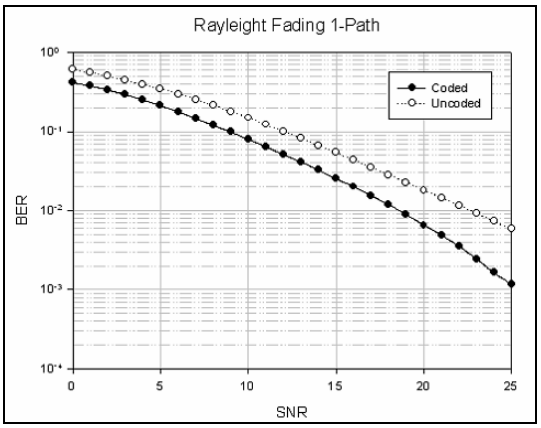


Fig. 15: BER Performance in Rayleigh fading channel

### 3.3. Performance Analysis of cdma2000 Modem

In this section we demonstrate the performance of our cdma2000 modem. The assumptions for performance analysis are listed below:

1. Frame structure: cdma2000 forward link, 4.8 kbps & 9.6 kbps fundamental channel
2. Error correction coding: convolutional code R=1/2, K=9
3. Frame error detection: cyclic redundancy code (CRC)
4. Orthogonal code: length-128 Walsh code
5. Channel environment: AWGN
6. Sampling rate: 1.2288 MHz, 6 bits per sample
7. ADC: 6-bit sample, 1.2288 MHz sampling rate.

Fig. 16 illustrates the BER performance for 4.8 kbps and 9.6 kbps as a function of chip energy (Ec) to noise energy (No). The spreading gains for 4.8 kbps and 9.6 kbps are 256 is 128, respectively. Notice the 3 dB performance difference for the two data rates. The BER performance improves as the spreading gain increases [10].

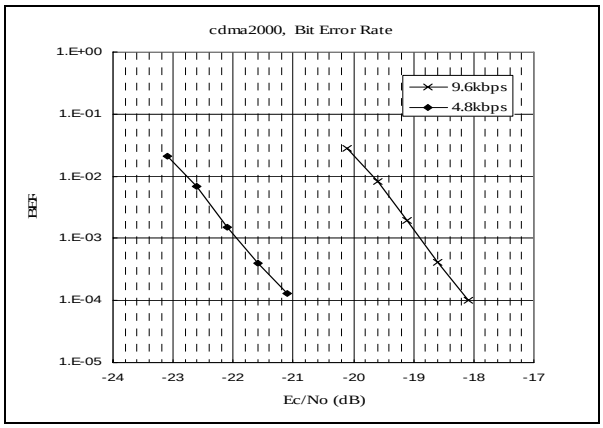


Fig. 16: BER performance in cdma2000 mode

Fig. 17 shows the frame error rate (FER) performance for 4.8 kbps and 9.6 kbps. Note that the FER performance improves as the spreading gain increases.

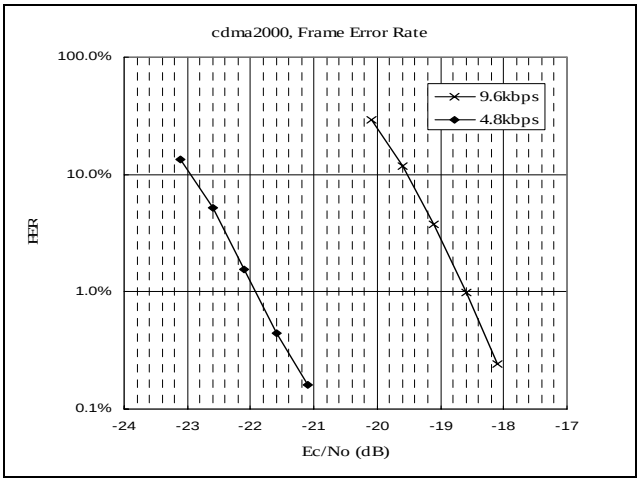


Fig. 17: FER performance in cdma2000 mode

## 5. CONCLUSION

We describe the design procedure of a triple-mode SDR handset modem which supports HSDPA, WiBro and cdma2000 mode, based on programmable devices such as DSPs and FPGAs. We analyzed the performances of each mode through experimental tests to verify the design of handset modem.


### ACKNOWLEDGMENT

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