NEW FPGAs BOOST SOFTWARE DEFINED RADIO PERFORMANCE

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ABSTRACT

With the advent of software defined radio platforms in military aerospace and now more recently in some consumer radio and electronics segments, the usefulness of field programmable logic (FPGAs) as reprogrammable digital signal processing (DSP) engines for SDR is taking on increased importance.

With recent advances in chip technology, not only is the silicon much faster and denser, but the fundamental role of the FPGA is changing dramatically. Indeed, DSP capability has become one of the most significant assets of the FPGA, as evidenced by sharp increases in engineering and marketing investments in this technology on the part of FPGA vendors over the last few years.

This paper discusses how FPGA technologies are being exploited in next generation COTS real-time software radio systems. Comparisons of various families of Xilinx FPGAs include details on specific features and important tradeoffs in performance, power consumption, signal integrity, serial interfaces, memory, speed and more. A real-life FPGA-based software radio transceiver system example is also presented. This paper will aid engineers in selecting the most appropriate FPGA to meet their software radio application needs.

1. FPGAS AND SOFTWARE RADIO

For many years, hardware design engineers have taken advantage of FPGAs (field programmable gate arrays) for connecting high-speed software radio peripherals like wideband A/D and D/A converters, digital receivers and communication links to programmable processors in embedded real-time systems.

FPGAs are especially well suited to handle the clocking, synchronization, and the other diverse timing circuitry needed to tame these specialized devices. In addition, FPGAs are excellent for data formatting tasks like serial-to-parallel conversion, data packing, time stamping, multiplexing, and packet formation.

With shrinking die geometries and other advances in chip technology, FPGA silicon became much faster and denser. But more importantly, the addition of new high-performance DSP resources marked a watershed event that dramatically changed the architectural paradigm of software radio systems. FPGAs are now incorporated in software radio products primarily for their DSP capabilities, thus stealing the spotlight from the more mundane traditional roles that they still serve admirably.

Without exception, the latest device offerings from major FPGA vendors offer second or third generation DSP blocks. These high-performance engines include extended precision multiplier/accumulators, advanced arithmetic units, logic engines, and flexible memory structures that can be tailored into block memory, dual-port RAM, FIFO memory and shift registers.

While these DSP capabilities of new FPGAs are truly remarkable, several other significant features add even more benefits to software radio applications. On-board serial gigabit transceivers and channel coding/decoding engines support the emerging switched serial fabric protocols that are quickly replacing conventional parallel buses and backplanes for high speed inter-chip and inter-board data transfers.

Other new features include on-board programmable RISC processors that can execute code for local supervision and control functions, thus greatly reducing the need for an external host processor. These processors slash loop latencies to deliver much tighter real-time control systems. Finally, Ethernet MACs (media access controllers), incorporated as I/O resources for the latest generation FPGAs, simplify TCP/IP communication links to a wide range of host processors and various operating systems.

2. NEW FPGA DEVICE FEATURES

Competition for design wins is stronger than ever, leading to an exciting race among FPGA vendors for features that deliver maximum performance and specific benefits. Winning this race, however, is a complex and elusive goal. With so many different types of resources – block RAM, distributed RAM, DSP blocks, logic blocks, micro-controllers, gigabit ports, I/O drivers and pins, etc – balancing a single optimum ratio is futile because each application requires a different blend. For example, the design engineer selecting the best part for a logic-intensive application will avoid an FPGA heavily burdened in cost and power with a wealth of powerful DSP blocks. As a compromise, vendors have developed multi-pronged product offerings, each targeting different classes of applications.

One example of such a family is the Xilinx Virtex-4 FPGA. Unlike the previous Virtex-II Pro family, Xilinx has split the seventeen Virtex-4 product offerings into three sub-families, each emphasizing distinct strengths. For the recently announced Virtex-5 family, there are a total of four distinct sub-families, but detailed information on only the first of these has been made public to date.

The Virtex-4 uses a 90 nm process and a core voltage of 1.2 volts, while the Virtex-5 shrinks the feature size down to 65 nm and drops the core voltage down to 1.0 volt. This allows an improvement in maximum clock speed to 500 and 550 MHz, respectively, while reducing power consumption.

Configurable Logic Blocks (CLBs) are the basic elements used for implementing state machines, combinatorial logic, controllers, and sequential circuits. They are composed of logic "slices" with flip-flops, look-up-tables (LUTs), multiplexers, Boolean logic blocks, and adder/subtractors with carry-look-ahead functions. The Virtex-5 uses 6-input LUTs instead of the 4-input LUTs in the Virtex-4, providing additional logic functions, fewer levels of logic for faster speed and less power due to simpler routing.

Memory has become much more flexible in these latest generation FPGAs and comes in different forms. Distributed memory is used for LUTs, FIFOs, single- and dual-port RAMs, and shift registers. For larger memory structures, 18-kilobit block RAMs can be used for deep FIFOs, large circular delay memory buffers, deep caches, as well as bigger single- and dual port RAMs. The Virtex-5 offers both 18- and 36-kilobit block RAMs to support wider memory structures of up to 72 bits within a single block.

One of the more significant advances in the Virtex-4 family is the new XtremeDSP slice. Following the market demand for more powerful signal processing structures, Xilinx surrounded the popular 18x18 hardware multipliers first introduced in the Virtex-II series with a 48-bit adder/subtractor capable of acting as a registered accumulator. Due to tight, dedicated logic, this facility can operate at clock speeds up to 500 MHz and can propagate the results between XtremeDSP slices with 48-bit precision at the same rate.

	Virtex-4 LX Devices			Virtex-4 SX Devices		Virtex-4 FX Devices			Virtex-5 LX Devices		
Sub-Family Specialty	LOGIC			DSP		MULTI-PURPOSE			LOGIC		
Product No. XC	4VLX60	4VLX100	4VLX200	4VSX35	4VSX55	4VFX60	4VFX100	4VFX140	5VLX85	5VLX110	5VLX330
Process Geometry	90 nm	90 nm	90 nm	90 nm	90 nm	90 nm	90 nm	90 nm	65	65	65
Core Voltage	1.2 v	1.2 v	1.2 v	1.2 v	1.2 v	1.2 v	1.2 v	1.2 v	1.0 v	1.0 v	1.0 v
CLB Logic Cells	59,904	110,592	200,448	34,560	55,296	56,880	94,896	142,128	82,944	110,592	331,776
Look Up Table Inputs	4	4	4	4	4	4	4	4	6	6	6
XtremeDSP Slices	64	96	96	192	512	128	160	192	--	--	--
DSP48E Slices	--	--	--	--	--	--	--	--	48	64	192
Multipliers	18 x 18	18 x 18	18 x 18	18 x 18	18 x 18	18 x 18	18 x 18	18 x 18	25 x 18	25 x 18	25 x 18
Distributed RAM (kbits)	416	768	1392	240	384	395	659	987	840	1120	3420
Block RAM/FIFOs	160 x 18	240 x 18	336 x 18	192 x 18	320 x 18	232 x 18	376 x 18	552 x 18	96 x 36	128 x 36	288 x 36
Total Block RAM (kbits)	2,880	4,320	6,048	3,456	5,760	4,176	6,768	9,936	3,456	4,608	10,368
Digital Clock Managers (DCM)	8	12	12	8	8	12	12	20	12	12	12
Phase-matched Clock Dividers (PMCD)	4	8	8	4	4	8	8	8	6	6	6
Max Differential I/O Pairs	320	480	480	224	320	288	384	448	280	400	600
PowerPC™ Processor Blocks	--	--	--	--	--	2	2	2	--	--	--
10/100/1000 Ethernet MAC Blocks	--	--	--	--	--	4	4	4	--	--	--
RocketIO™ Serial Transceivers	--	--	--	--	--	16	20	24	--	--	--
Configuration Memory (bits)	18315K	31818K	50648K	14476K	24088K	22262K	35122K	50900K	21800K	29100K	79700K
Max SelectIO™	640	960	960	448	640	576	768	896	560	800	1200

Figure 1. Major Resources for Representative Devices from Virtex-4 and –5 Sub-Families

The 48-bit path allows this fast, fixed-point hardware to rival the precision of floating-point engines by preserving the 36-bit multiplier outputs with plenty of overhead for bit growth as results propagate through cascaded slices.

Each XtremeDSP slice features 40 dynamically controlled logical and arithmetic modes and supports mode changes during runtime without the need to recompile the FPGA. In this way, each XtremeDSP slice behaves like a miniature DSP processor, and there are as many as 512 of these in a single FPGA.

With so much demand for DSP capability, the Virtex-5 family features the DSP48E slice that boosts 18x18 hardware multiplier to 18x25 so that single-precision floating-point arithmetic can be implemented within two DSP48E slices instead of the four slices required with the Virtex-4 XtremeDSP. Also, the adder has been enhanced with a logic stage to save the need for an external logic block.

Twenty different user-configurable interface standards for the device I/O pins offer flexible connections to a diverse range of external hardware devices. New in the Virtex-4 and continued in the Virtex-5 is the active termination feature that not only provides programmable termination within the FPGA to drastically reduce the number of external discrete resistors, but also dynamically adjusts termination impedance to track changes in drive levels due to process, temperature and device variations.

Source-synchronous interfaces include serializer/deserializer blocks that match faster data rates on external data buses to slower, wider buses inside the FPGA to help reduce power. Interfaces to a wealth of fast external memory devices include DDR and DDR2 SDRAM, QDR and QDR II SRAM, and RLDRAM II. These interfaces are made easier with programmable clock and data skew circuitry to match complex setup and hold time requirements.

Digital clock managers allow different regions of the FPGA to be operated at different clock frequencies that can be synchronized from various external clock references. Frequency synthesizers with multipliers and phased-matched clock dividers precisely align external timing signals with data sources and destinations.

3. SUB-FAMILY DIVERSITY

All of the resources described so far are available in all Virtex-4 and Virtex-5 devices, but the ratio of these resources differs significantly among the sub-families. Figure 1 shows the relative strengths of resources for each of the three Virtex-4 sub-families and the LX sub-family of the Virtex-5 for the larger devices in each group.

The LX sub-families for the Virtex-4 and Virtex-5 deliver the most logic and I/O. The Virtex-4 SX sub-family aims at DSP with 512 XtremeDSP slices, and the FX sub-family offers generous memory and three other important resources found only in FX devices.

The first of these are on-board IBM 405 PowerPC processor cores that can be used as local micro-controllers to implement complete systems on a chip, often eliminating the need for an external CPU for high-level supervisory functions.

The second resource is a set of serial gigabit transceivers capable of handling bit rates up to 10 GHz and backed up with serializer/deserializer logic. By configuring these interfaces through available IP cores, the FPGA supports popular high-speed serial standards and switched serial fabrics including Serial RapidIO, PCI Express, FibreChannel, SATA, SONET, and many others.

The third resource unique to the FX family is a set of 802.3 compliant Ethernet media access controllers (MACs). These support 10/100/1000 Base-x transmit/receive interfaces to system peripherals, and are especially useful to the embedded PowerPC processors as a standard communication link to the outside world.

While no Virtex-5 sub-families beyond the LX devices have been announced at this time, it is logical to expect that enhanced versions of these last three resources will be found on at least some of the future sub-family offerings.

4. BENEFITS FOR SOFTWARE DEFINED RADIO

It is clear that each one of these many resources offers a direct benefit for software radio systems for all of the many functions summarized below:

- Interfacing to ASICs including A/Ds and D/As
- Digital down converters (DDCs) and digital up converters (DUCs)
- Modulating and demodulating for precise frequency spectrum utilization
- Encoding and decoding for complex multi-channel standards
- Encryption and decryption for secure communication
- Signal identification and tracking using FFTs and adaptive control loops
- Receive and transmit beamforming for directional control and signal enhancement
- High-speed interconnects between devices and between system components
- Localized high-level control using on-board processors for autonomous operation
- Simplified communication to host networks using on-board Ethernet MACs

5. SOFTWARE RADIO PRODUCT EXAMPLE

Harnessing these resources for a high-performance software radio product illustrates the usefulness of the sub-family differentiation. The product shown in Figure 2 is the Model 7142 PMC (PCI Mezzanine Card) module suitable for use in many different types of embedded computer systems, including PCI, VME, and CompactPCI card cages. The new XMC extension to PMC defined by VITA 42 offers gigabit serial links supporting the new popular switched fabric protocols.

XtremeDSP slices as one of the smaller SX devices. Since customer access to ample DSP horsepower was a critical factor, an SX55 device was added to the PMC module, significantly boosting the total quantity of DSP slices from 192 to 704.

Once the SX55 was enlisted for service to handle real-time digital signal processing for the A/D, D/A, and SDRAM, those peripherals were attached directly to it by choosing the most appropriate interface type. Therefore, the FX100 became the natural candidate for the PCI interface, DMA controller and gigabit serial interface.

The PCI interface incorporated an off-the-shelf IP core installed in the FX100 to speed development time and to ensure full compatibility with all PCI 2.2 PCIbus specification. Because of the many different peripherals and devices, the local side of the PCI core is augmented with a custom 9-channel DMA engine and FIFO buffers. This provides a dedicated logical channel to and from the PCI bus to manage multiple streams and simplify transfers.
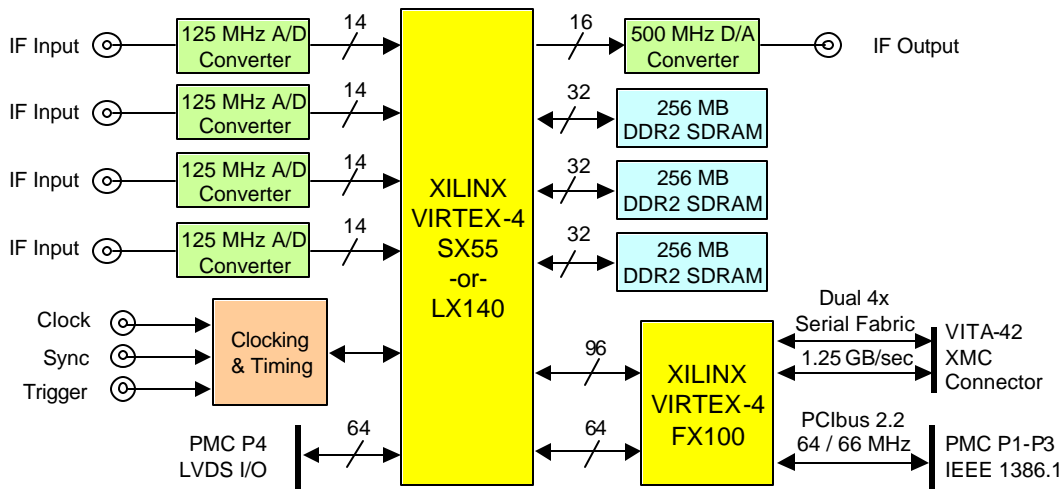

Figure 2. Model 7142 Virtex-4 Software Radio PMC/XMC Mezzanine Module

Four 125 MHz 14-bit A/D converters and one 500 MHz 16-bit D/A converter provide analog IF (intermediate frequency) signal interfaces to external analog RF up and down converters and RF amplifiers for ultimate connection to the antenna. Real-time digital signal processing tasks such as digital up and down conversion, modulation and demodulation, encoding and decoding, and other operations are often all performed using FPGA -based DSP resources.

As a PMC module, a PCIbus interface must be provided along with DMA controllers and FIFO buffers to move data efficiently between the PCI bus and the many peripherals on the module. As an XMC module, the unit must include gigabit serial transceivers and some facility for implementing a serial fabric and/or protocol.

Delivery of the Model 7142 was required prior to Virtex-5 device availability, so the Virtex-4 family was chosen to meet the module requirements. Since only the versatile FX sub-family provided all of the necessary features, it becomes an obvious choice for this product.

Nevertheless, the FX family is quite limited in DSP capability compared to the SX family. Even the largest member of the FX family has only the same number of

simplify transfers.

Three 256 MB DDR2 SDRAMs support circular buffers for implementing digital delay memories, which are very useful in signal intelligence applications. These memories can also be used for capturing transients from the A/D converters for radar signal acquisition, or for storing waveforms that can be played in real-time out to the D/A converter to create an arbitrary waveform generator. A third-party SDRAM controller IP core was installed to manage the critical clock, control, data and address interfaces, thereby eliminating that chore from the design effort

The RocketIO gigabit serial interfaces of the FX were organized into two groups of four bi-directional serial bit lanes to form two "4x" ports. Backup up by the internal 8b10b channel coding circuitry, these ports from the physical and transport layers of XMC standard. IP cores can be installed to implement for specific switched fabric standards including SerialRapidIO, PCI Express and others. Operating at bit clock rates up to 3.125 GHz, and soon 6.25 GHz, these I/O facilities eliminate many of the data flow bottlenecks that frequently plague real-time embedded systems.

Joining the two FPGAs are two parallel data buses. The 64-bit path supports traffic to and from the PCI interface sustaining rates up to 133 MHz. Three 32-bit buses use source synchronous digital interfaces for moving data between them at up to 600 MHz to support the full 2.5 GByte/sec streaming transfer rate of the XMC ports.

By judiciously choosing Virtex-4 sub-family members to meet specific needs of the hardware and application, all initial design objectives were nicely satisfied. An additional bonus arises from the "footprint" consistency between certain members of different Virtex-4 sub-families. Since the SX55 and the LX100 share a common printed circuit board pattern, or footprint, this module can be assembled with either device. For applications requiring maximum amount of logic resources, the chart in Figure 1 shows that the LX100 doubles the number of logic slices over the SX55.

6. SUMMARY

Because software radio technology drives such a diverse array of commercial, industrial, military and government electronic systems, the new features and inherent flexibility afforded by FPGAs deliver an excellent solution. The increasing quality and quantity of IP core offerings for highly-optimized algorithms, interfaces, and protocols help COTS board vendors shorten their time to market, and help systems integrators add critical functions to these FPGA-based COTS products for specialized turnkey applications. EDA tool vendors race to digest and tame the increasing complexity of these new hardware offerings, and compete with each other in reducing design time, improving design integrity, and maintaining portability to next generation devices.