UNDERSTANDING STATE-OF-THE-ART IN ADCS

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ABSTRACT

Enabling technologies are reaching a pivotal point where efficient Software Defined Radios (SDR) may soon become a reality in many marketplaces. One of these technologies is the analog-to-digital converter (ADC) which is often the performance-limiting element in such systems. New converter architectures and processes are helping to improve critical performance; what was at one time not possible can now be achieved. New converters are also renewing interest in old receiver architectures to provide increased flexibility and simplicity. While IF sampling systems have gained popularity in recent years, focus is often towards direct conversion architectures for both transmit and receive paths. This paper examines where converters are and where they are headed in terms of enabling performance. In regard to performance, the types of receiver architectures that are enabled by this performance and how this can simplify the implementation of SDR technologies are examined along with the some of the many tradeoffs between the different topologies. While typical characteristics such as SNR and SFDR are examined to see how they affect system performance, other more subtle converter behavior characteristics that have always existed are examined closely to see how they may affect transceiver performance.

1. INTRODUCTION

Walden [1] and others have extensively written on the progress of data converters over the recent decades. These are often insightful and educational [2]. In either case, they are from the perspective of an end user and often miss the motivations and limitations that drive and curtail developments of the next generation of converters. In a general sense, the accelerants are market demand (primary application) and the inhibitors are process and architecture. In fact, in most cases it is the innovation through a hindrance that enables the next level of performance.

For example through the early 80's radar and instrumentation applications constantly pressed state-of-the-art in ADCs as high precision converters moved from PCB sub-systems into Hybrid technology. However, because of the high cost of these manufacturing technologies, actual ADC volumes were quite low. Eventually, the semiconductor technology reached a point in the mid-1990's where monolithic ADC performance was similar to that of hybrid devices, thereby dropping the cost of ADC systems by an order of magnitude. This trend continued as consumer demand for personal computers drove the cost of manufacturing all semiconductors downward, including that of ADCs.

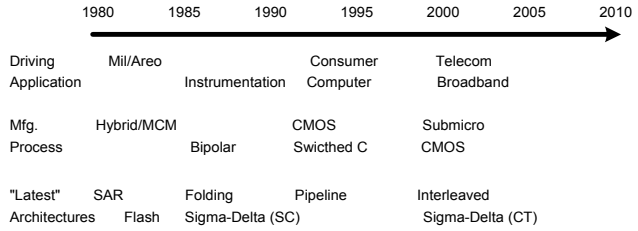

Figure 1. Time table of ADC developments

As costs fell and performance increased, ADCs became one of the enablers for the rapid growth and advances in wireless and digital telecommunications. Today, telecommunications designers are stretching the limitations of available converters and are looking for clues as to where to look next as there is a direct link between converter performance and receiver architectures. While past performance is not always an indicator of the future, it is as good an indicator as any other, especially in light of the fact that last generations hindrances often produce the next generation's enablers as converter designers' work to improve performance.

2. ROLE OF HISTORY

Telecommunications has not been the only driver for ADCs. For several decades RADAR applications drove converter requirements. During this period, specifications such as transient response and over-voltage recovery were paramount along with phase linearity. Instrumentation customers were also eager for devices with good step responses in order to faithfully digitize the fast edges of a plethora of waveforms.

As compact converter subsystems became available in the 1970's a variety of industrial applications developed. Typically these were closed-loop systems where the ADC was used as part of the sense loop. In control applications, static linearity of converters was important for the loop respond to linearly to the stimulus. In addition to specifications such as INL and DNL, a key requirement of these applications was 'No Missing Codes' and

monotonicity. If the converter transfer function was not monotonic or consisted of missing values, the localized slope of the converter became inverted and the loop became unstable.

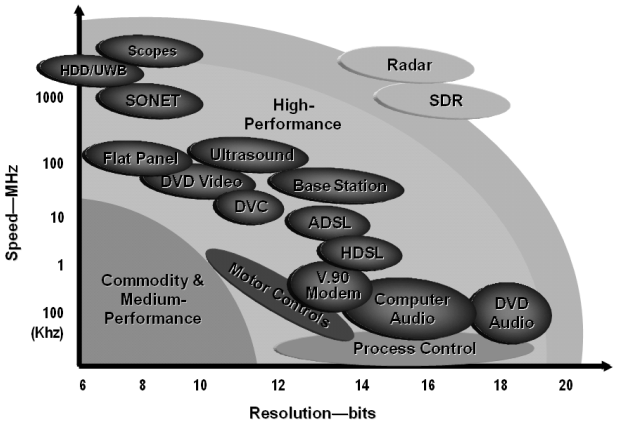

Figure 2. Commercial ADC Drivers

Until around 1993 these applications drove converter improvements. As with any cutting edge technology, advances in one area tend to pull other technologies along as well. Data converters in general have long been associated with the telecom industry at least as far back as the 1930's [3]. In the early days of telephony, conversion from analog-to-digital was a potential means of reducing transmission noise and increasing call capacity. Eventually it provided a method to ensure integrity and security but resulted in the requirement for even higher levels of performance, further driving the levels of performance. Technologies such as direct sequence spread spectrum took advantage of correlation as a means of recovering a signal buried within thermal noise. While sensitivity in a receiver has always been an issue, contemporary demodulation schemes have sought to push the noise floor of data converters continually lower.

It is interesting to review the brief history of applications and how they drive converter specification because nearly all commercial data sheets contain vestiges of these specifications. Although many of these early specifications are still important, they are not as meaningful in modern communications applications as others. For example, 'No Missing Codes' or 'guaranteed monotonic' means little for high speed converters that typically have several fewer effective number of bits (ENOB) than the converter resolution. Similarly, many audio codecs are notoriously non-linear with respect to their total resolution, yet meet the demanding low distortion and noise requirements of audiophiles. These specifications often remain on contemporary converter data sheets as a testament to how the early applications shaped the evolution of converters.

Therefore, it is clear that contemporary applications will directly affect all aspects of converter performance in future generations. It is incumbent on academics and commercial users to maintain communications with and direct manufactures of converters in exactly what specifications are important and what they need to be. Unfortunately, many consider their end application requirements proprietary or due to insufficient engineering resources fail to appreciate what the full requirements of their converters must be and often either over or under estimate true needs.

3. ROLE OF PROCESS

As converters became widely available, the general rule was to use what ever technology that was available that gave the best performance. This was most noticeable when ADCs were widely available as PCBs, modules, MCMs or hybrids. During this period, the designer was able to pick and choose the individual technologies in order to optimize performance. This was necessary until mainstream semiconductor processes were available in the mid 1970's [3] that were suitable for mixed-signal designs and continues today on a smaller, more specialized scale.

During this period it was common for these processes to be proprietary and optimized by the companies using them especially for the manufacturing of data converters. Many times these processes were tweaked and optimized on a product-by-product basis to achieve the specified level of performance. While this is not common for production converters today, it is often the case for experimental devices seeking maximized performance, or when verifying the effects of process variation on performance. At present, proprietary processes are still used for many competing devices where one dimension or another is optimized such as speed, SNR or high voltage operation.

More common today is the use of commodity CMOS processes. These processes are widely available, inexpensive and provide high yield. While these processes yield high quality product in high volumes, they are not generally optimized for analog and mixed-signal designs. In order to provide high analog performance on these processes, designers have to be very innovative, not only in their circuit design but also in their architecture, trading off minimum feature size for optimized analog performance. As a result, while digital products follow Moore's Law on ever shrinking processes, analog products follow at a much slower rate [4]. Evidence towards that end is seen in the plot of ISSCC papers given in various fine-line geometries by year. Interestingly, the table clearly shows that each geometry has a definitive peak over the last 6 years. Even more interesting is that 0.25 um was skipped almost

entirely, and the same appears to have occurred for 0.13 um as well.

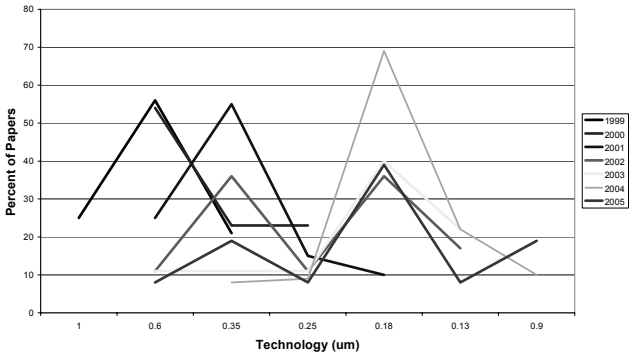

Figure 3. Percentage of ISSCC Papers by process

One thing is clear from recent trends: CMOS has been a significant factor in reducing the cost and power of converters. This has enabled many new applications in the consumer, communications and other areas but it has not lead to significant levels of improvement in figures-of-merit outside the area of power. Improvements in figures-of-merit have historically been seen in products manufactured on proprietary or analog optimized processes such as bipolar, Bi-CMOS or more recently on SiGe or GaAs. This trend is likely to continue with performance optimized on custom processes, and price/power optimized devices on commodity CMOS. This is not to say that CMOS products will not improve -- indeed they will. However, their performance will likely follow that of those manufactured on proprietary processes.

4. ROLE OF ARCHITECTURE

The role of the ADC architectures is that of enabler for the required specification. As pointed out by Le and Rondeau [2], certain converter architectures are optimized for certain parameters. For example, Sigma-Delta architectures are optimized for power efficiency while Flash converters are optimized for speed. Various other architectures are optimized for varying combinations of speed, dynamic performance such as SNR and SFDR and power. Therefore, it is by the selection of the architecture that individual specifications are often achieved.

As noted in the prior section, architecture is also pivotal in optimizing performance on a given process. Therefore an architecture that is optimal on one process may not be optimal on another. Nonetheless, the pipelined architecture is one of the more common for high performance; high speed converters because it allows tradeoffs between power, speed, and physical size, while maintaining a high degree of performance (see Le and Rondeau [2]). While new architectures continue to evolve, pipelined converters will continue to lead the performance curve because they allow for a wide range of optimizations across process and performance constraints. Other technologies such as SAR and sigma-delta will see increased usage, especially in integrated solutions, at the same time that their performance will increase. However, because of the over-sampling required in these architectures, they will not be overly useful in very high sampling rate applications for some time to come.

5. ROLE OF APPLICATION

These distinctions between pipelined and SAR or sigma-delta converters may well define the primary roles for these converters. Pipelined converters tend to have higher absolute sample rates for a given resolution, and therefore are ideal candidates for the popular IF sampling receivers; while SAR and sigma-delta converters typically have limited bandwidths, and are therefore well suited for baseband applications.

5.1. Baseband Sampling

A baseband sampling receiver is one that utilizes a pair of ADCs to sample an I and Q signal. Even within the context of SDR where signal bandwidths can vary, bandwidths are often well contained due to regulatory requirements. As such, lower sampling rate converters are suitable for many baseband sampling. Sigma-delta converters are often employed in integrated applications such as handsets applications because of their exceptional performance for limited bandwidth signals and their low power.

In these applications, typically as much noise and spurious performance is achieved as possible given the power budget and clocking rate. Because of the great flexibility of sigma-delta converters, they are easy to optimize for a wide range of requirements within the scope of clock rate and therefore find uses in many different applications. Recently, Successive Approximation ADCs have gained more popularity as in these applications as well and may see further development as commodity CMOS becomes further refined for analog signal processing.

A variation on the sigma-delta converter that does offer much promise is the band-pass sampling sigma-delta converter. Instead of sampling at baseband, the input is translated to a useful IF frequency. While the bandwidth remains limited, it does allow many of the properties of an IF sampling converter to be merged with those of sigma-delta technology. Implemented in continuous time technology, the front end resembles the tuned network of an LC filter found in all receiver topologies.

5.2. IF Sampling

An IF sampling receiver is one that utilizes the ADC to sample the analog signal before it is converted to baseband. In many cases this can be a low IF signal of only a few hundred kHz, but more often, the signal is several hundred MHz. By sampling at high IF frequencies, the ADC functions as a mixer-to-digits, subsequently eliminating the requirement for additional analog signal processing and mixers stages. Such architecture places heavy requirements on the ADC for a number of reasons.

In order to accurately sample high frequency signals, high analog bandwidths are required. In all traditional ADCs, the sampling mechanism is a capacitor and a switch. Because the switch has a finite resistance and the capacitor a finite value determined largely by process and architecture, a low pass filter is formed. Design optimization typically focuses on generating a switch with the smallest possible resistance. For wideband converters, the largest possible bandwidth is desirable and therefore the smallest value of capacitor possible is used. The wider the bandwidth, the more noise that enters the sampling process. Therefore, for a given design, SNR is inversely proportional to bandwidth. This is one of the key reasons why high bandwidth converters have fewer SNR bits than the total resolution of the ADC.

In addition to good SNR performance, IF sampling architectures require good spurious free dynamic range (SFDR) performance. Spurious performance is determined by both the static transfer function and the dynamic transfer function. Dynamic performance is limited largely by the slew rate limitations in the sampling circuit and any internal analog nodes that settle on a clock-by-clock basis. Therefore, the larger the capacitance associated with the sampling function, the worse the SFDR performance. Here lies the paradox for high speed converters used in IF sampling; there is a fundamental tradeoff between noise and spurious performance. Therefore, in order to achieve higher IF sampling, SNR must suffer at the expense of higher bandwidths. This basic tradeoff drives innovation in circuit design and process development as the fundamental limitations of each are discovered.

Lastly, the ADC must function as a mixer in IF sampling applications. Therefore, it must exhibit excellent phase noise characteristics. Not only that, but the clock used as the sample clock must exhibit excellent phase noise and low clock jitter [5]. All other issues aside with advancements in converters, clock path jitter alone can limit absolute performance. As pointed out in numerous references in the literature, converter noise limitations due to jitter are directly proportional to clock jitter and analog frequency. Therefore, recent advances in reducing converter jitter have yielded significant improvements in converter noise performance [6]. While Walden labels jitter improvements as spotty, it is often a function of rotating priorities. Only after his publication, did IF sampling achieve enough commercial success to drive reduction of converter clock jitter nor were the design tools available to aid the designers' reduction of such noise. Despite all of the challenges to IF sampling receiver architectures, they have become quite popular in recent years. This is largely due to the fact that digitizing earlier in the signal chain allows many of the analog signal processing blocks to be omitted, yielding a more stable and potentially cheaper design that enables both SDR and other flexible radio architectures.

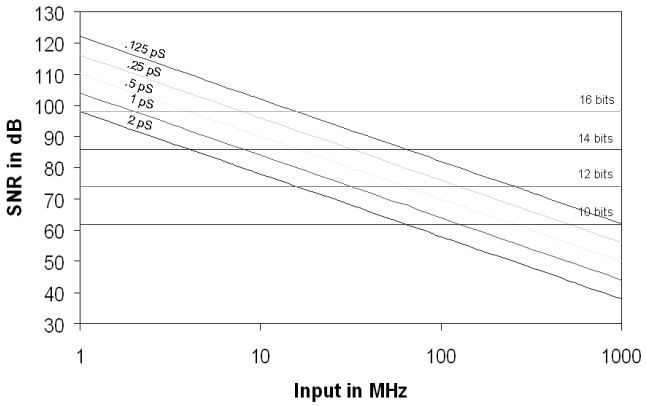

Figure 4. Clock Jitter requirements for ADCs

The logical extension of IF sampling is direct RF sampling. While there are many reasons to consider such a solution, the technical challenges are great. In direct RF sampling applications, there is little analog signal processing between the antenna and the converter. Therefore, the ADC must exhibit a low noise figure while also maintaining linearity in the presence of large adjacent or out-of-band signals. A key advantage to superhet radio designs is the ability to balance these two requirements across multiple stages. With direct RF sampling no such stages exist and the converter must support the full dynamic range. While much interest exists in this topology, successful applications will require a careful balance between input noise and input blocking. Some applications will emerge, but in the context of SDR where a wide range of input conditions must be tolerated, other more traditional architectures such as IF sampling and baseband sampling may provide better performance.

6. CRITICAL PERFORMANCE TRENDS

There are a number of performance metrics followed for data converters. While they exist in a number of formats and fashions, it is interesting to examine them to see how they change as a function of time.

6.1. Power Dissipation

One of the more interesting issues to examine is that of power dissipation. Although usually not considered directly as a performance metric, power does factor into most ADC figure-of-merit calculations in the dominator, indicating that the lower the power, the better the figure-of-merit. In the following figure, power versus time periodically experiences rapid declines followed by a period of relative stability. Note in particular for the 10 bit 40 MSPS curves, the transitions years are 1989, 1995 and 1999. These inflections points correspond nicely with the emerging technologies/architectures of bipolar ICs, CMOS/Switched Capacitor ICs and sub-micro CMOS IC's respectively.

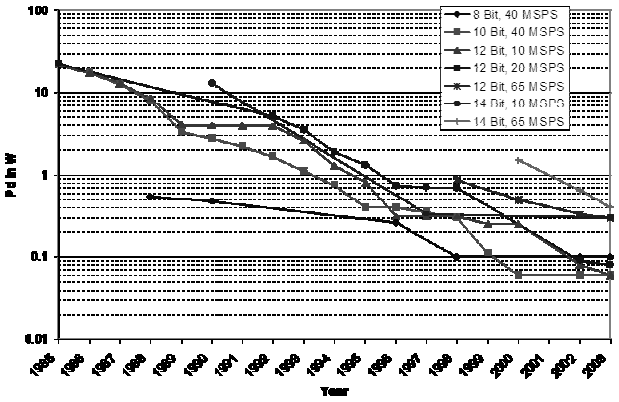

Figure 5. Power Dissipation vs. Time for ADCs

There are several points to note. First, different resolutions exhibit inflection points at different years for a number of reasons. For example, 6 bit monolithic flash converters were available well before 1985 but higher resolution flashes were not. Second, once a new process technology is established, circuit innovation drives the power down until a new technology arrives and causes significant drops. Finally, as analog size reduction slowly follows digital size per Moore's law, the inflection points should get closer together with little lag time before the impact shows up as new generations are adopted.

Looking back at the ISSCC papers by geometry, it is clear that 0.18 um CMOS is heavily impacting the power curve at present. Although it appears as if 0.13 may be skipped for data converters, future generations will take advantage of power savings from smaller geometries.

6.2. Converter Bits

There is always confusion when talking about converter bits. A converter has a physical number of bits that correspond usually to pins on the device. These are sometimes referred to as "marketing bits" or "resolution". However performance may or may not correspond to these physical bits. Typically, performance bits are fewer than the number of marketing bits. These bits are often called Effective Number of Bits (ENOB) or SNR bits.

As noted by Le and Rondeau in a current survey, converter performance in terms of figure-of-merit which is a derivative of SNR bits, have seen exponential growth over the last half decade which correlates very strongly with the power dissipation curve presented earlier and with the continued development of fine-line CMOS processes. As long as semiconductor processes continue to improve and refine, converter performance metrics will continue to improve. While Walden suggested 1.5 bits per 8 years, recent acceleration in performance in conjunction with increased competition between ADC manufacturers suggests a more rapid increase in performance in the future.

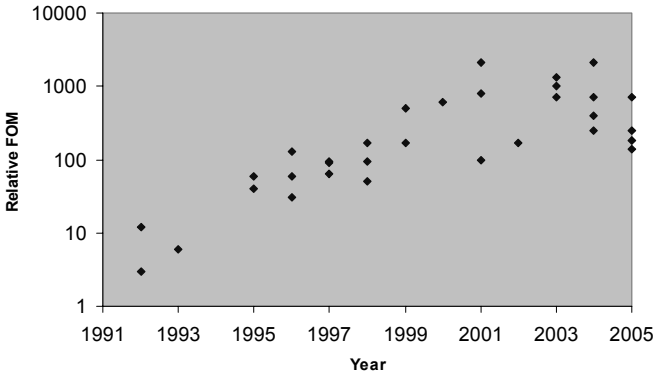

Figure 6. High Speed ADC Figure-of-merit

While this trend is obvious, it should be noted that the difference between the marketing bits and the SNR bits is increasing. This trend suggests that it is getting more and more difficult to continue to increase performance. As Walden reminds us, there is a fundamental limit beyond which we can not go. In converter terms, this is thermal noise. As the marketing bits increase, the weight of the LSB continues to approach the thermal noise limits for the design. While designers have some ability to minimize noise as mentioned earlier, there is only so much that can be done. To overcome these challenges, designers must innovate, realizing that there is a limit to how much converters can improve with current processes and architectures and look to future processes for additional gains.

7. MODELING

In order to fully optimize designs, users of ADCs should take full advantage of simulation tools. One of the most common mistakes is underestimating the impact the ADC has on overall system performance. This is understandable given that converter data sheets are often very confusing [7]. As mentioned earlier, data sheets often contain legacy specifications that may look enticing but in reality mean very little in the desired application.

A good converter model will faithfully conform to the behavior of the converter as a function both of frequency and amplitude. When incorporated with other devices in a system simulation, these models are useful at predicting issues with sensitivity, gain linearity and distortion products during blocking conditions specific to the desired application. It is not possible to extract from a data sheet how a device will perform in a given application unless the test conditions conform exactly to the end application. This is seldom the case.

For example, consider a wideband high IF waveform. Such a waveform may have a peak-to-rms value of 12 dB. If single tone testing is utilized to determine if the converter is suitable for a design, it will become obvious that the spurious performance may be inadequate. However, if the same converter is stimulated with a wideband IF signal of the same peak power, the rms value and hence the input slew rate will be much lower and overall performance will be much better. This is demonstrated in the following figure. Here a narrow band tone is plotted over a WCDMA modulated waveform. Both signals are stimulating the analog input of the converter at 190 MHz. However, the spurious terms of the modulated waveform are much lower due to the high peak to rms ratio. Additionally, note that the noise floor of the modulated signal is lower due to the reduced effects of jitter and high order distortion terms.

Although this is a simple demonstration of the benefit of observing the converter in the end application, it shows the advantage of including a good behavioral model of the ADC in system simulations. Converter models are available for many high speed converters and can greatly improve the performance prediction of system simulations, especially when analyzing the subtle behavior characteristics of complex communications applications.

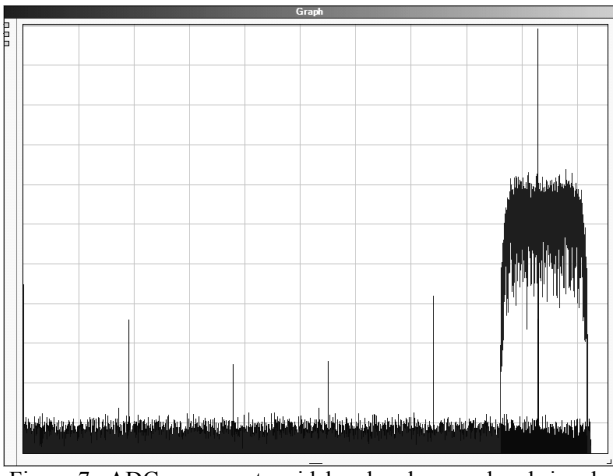

Figure 7. ADC response to wideband and narrowband signals

8. CONCLUSION

Selecting the right ADC for an application can be a daunting task. As seen in this paper, converters are continuing to improve in all aspects of performance and will continue to do so in the coming years. Unfortunately, performance increase often comes sporadically as designers have to innovate through various obstacles. However, it is clear that despite a general lag behind advances in digital processing, ADCs are nonetheless rapidly improving in all areas of figures-of-merit and will continue to do so, at least in the foreseeable future. Many exciting possibilities are just around the corner as new substrate materials offer methods to enable increased performance in the future. As this happens, converter manufacturers must work closely with the system designers so that proper tradeoffs are made. Without this, improvements will be made, but not always in the direction needed by the application, nor at the desired pace.

9. REFERENCES

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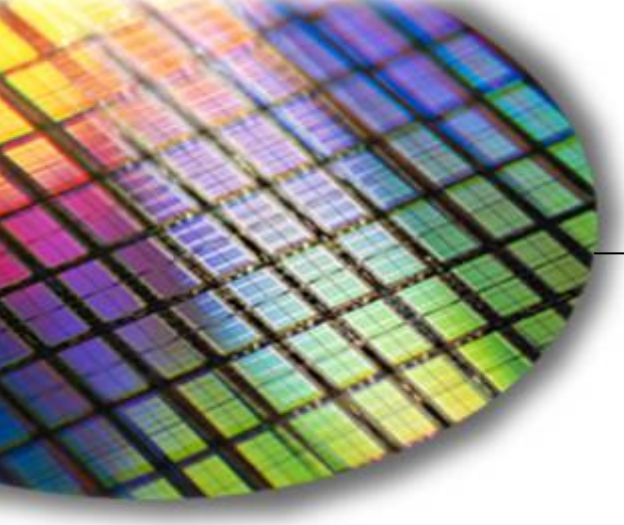

The World Leader in High Performance Signal Processing Solutions

Understanding State-of-the-art in ADCs

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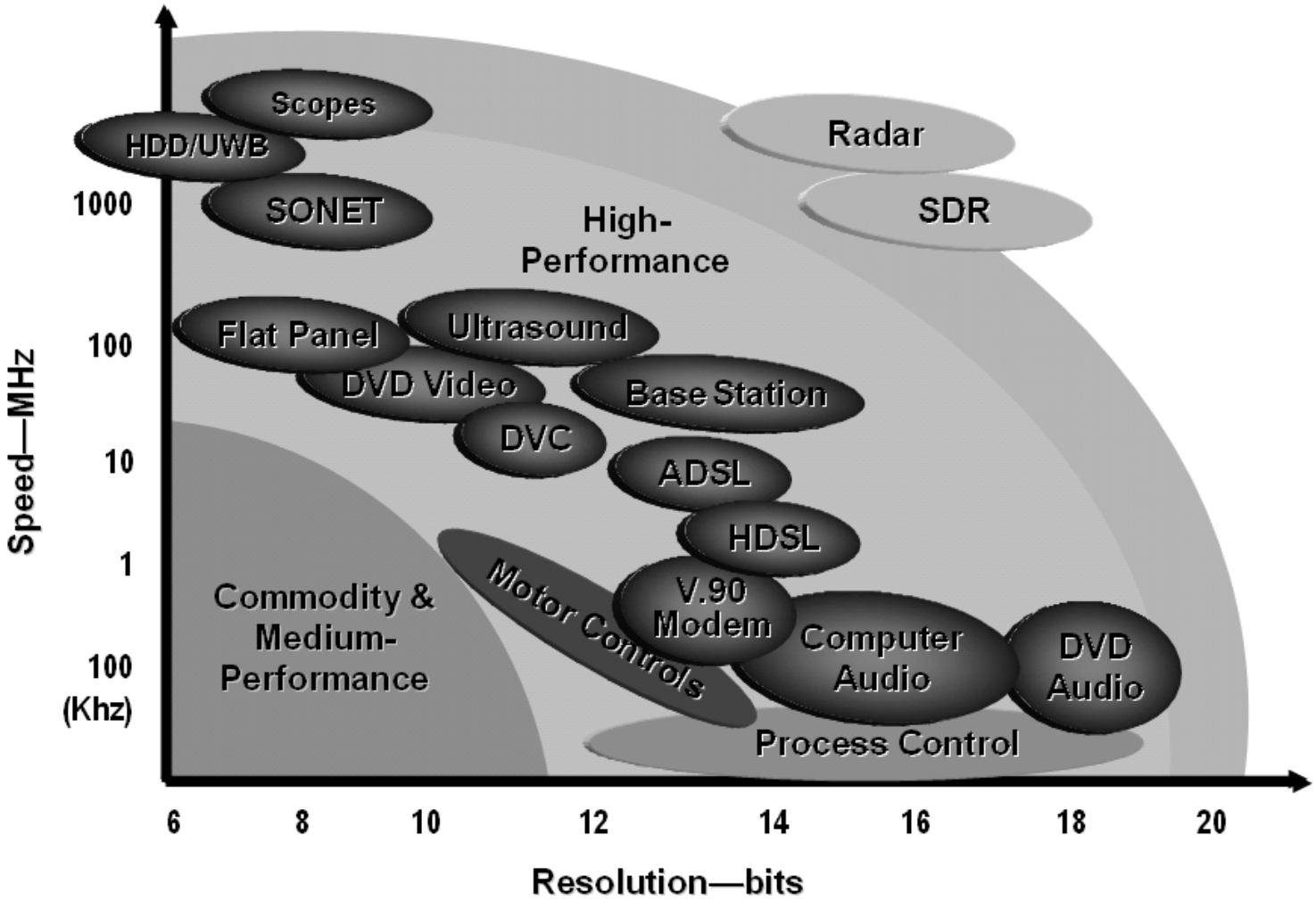
ANALOG DEVICES

Introduction

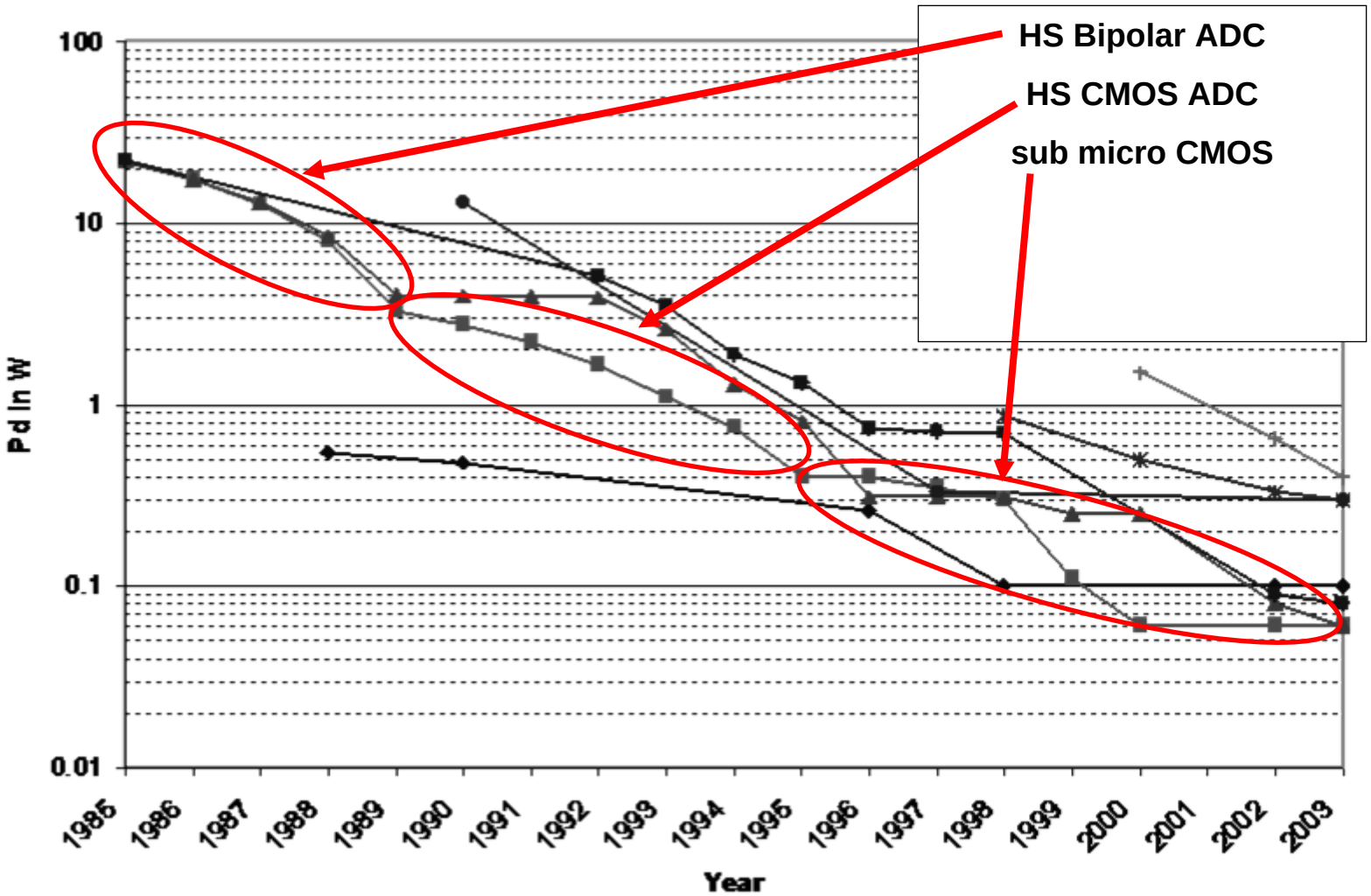


ANALOG DEVICES

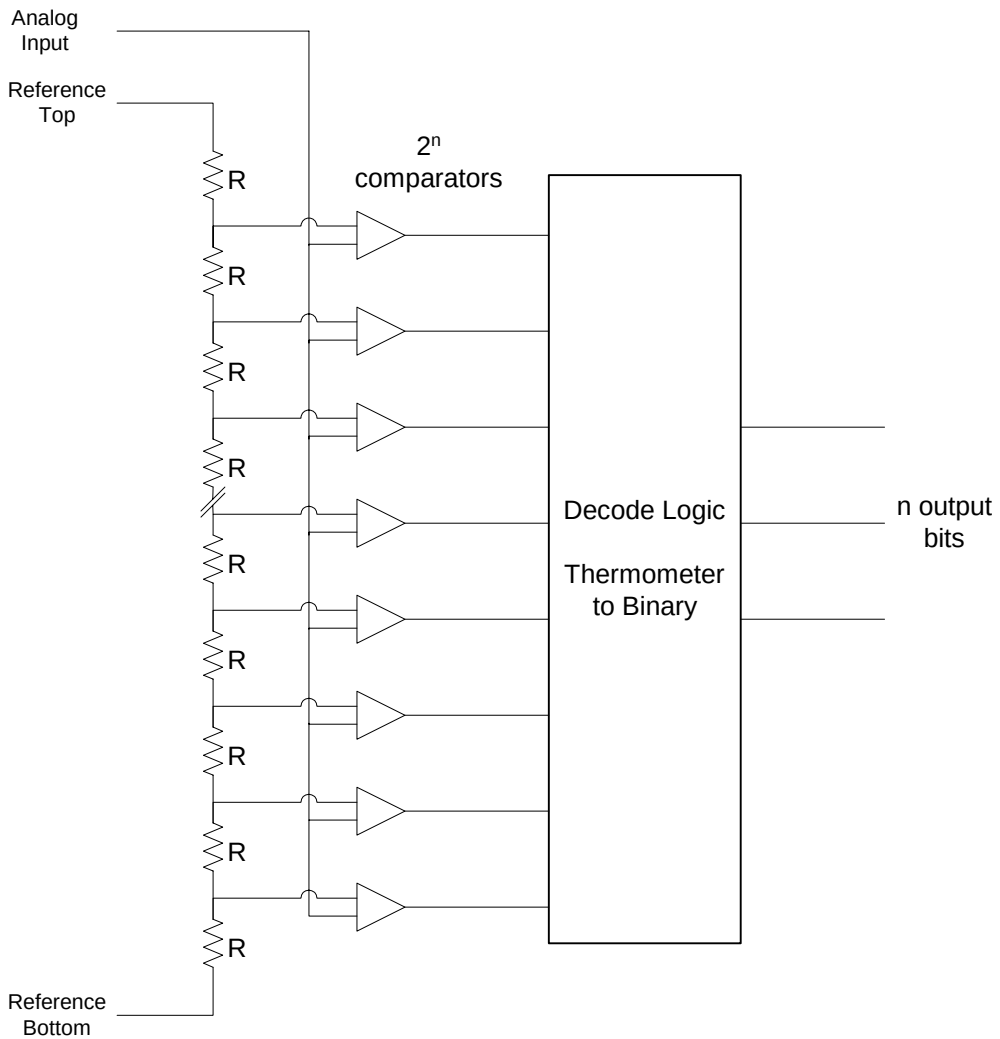
Role of History

Driving Application	Mil/Areo		Instrumentation	Consumer Computer		Telecom Broadband
Mfg. Process	Hybrid/MCM		Bipolar	CMOS Swicthed C		Submicro CMOS
"Latest" Architectures	SAR	Flash	Folding Sigma-Delta (SC)	Pipeline		Interleaved Sigma-Delta (CT)

Role of Process



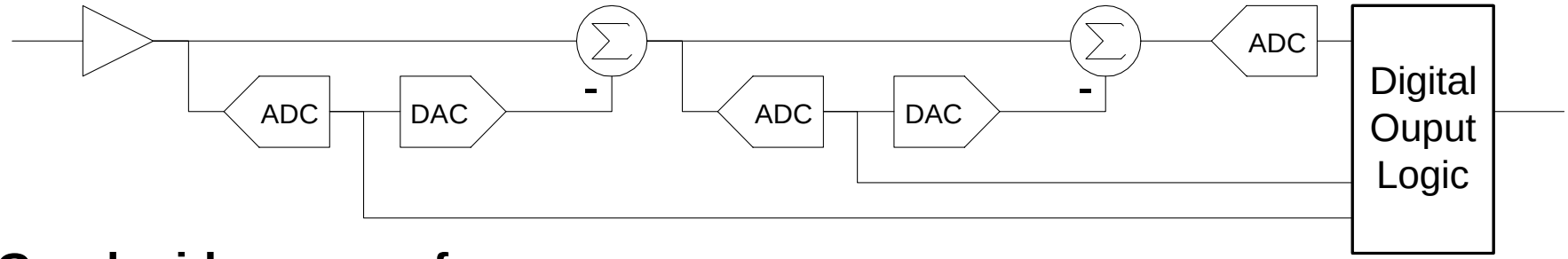
Role of Architecture: Flash Converters



- **Really good for low resolution (<10 bits)**
- **Really good for very high sample rates (into GHz range)**
- **Baseband and IF sampling applications (even RF)**

- **Complexity grows exponentially with the number of bits**
  - **Need 2^N comparators**
- **So does power**
- **The input is very capacitive**

Role of Architecture: Pipelined or Subranging Converters



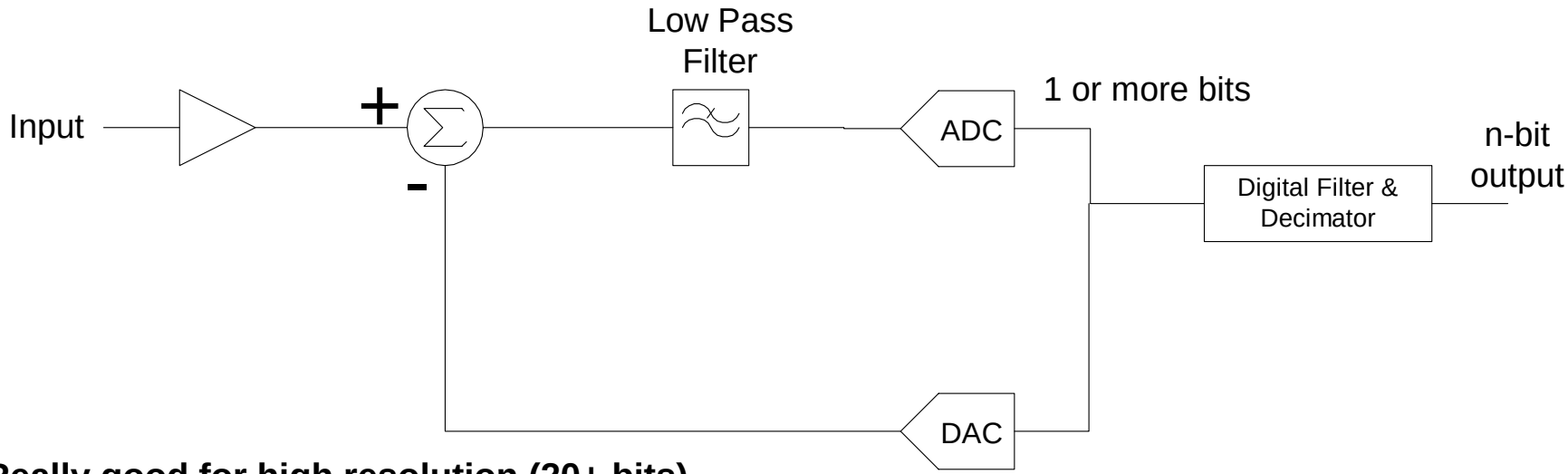
Good midrange performance
- High Resolution (16+ bits)
- High Speed (Hundreds of MHz)
- High BW (Hundreds of MHz)

Speed and BW limited by chip delay and internal settling times.

Thermal noise limits potential SNR
- Due to the number of cascaded stages
- Due to the wide bandwidths

Spurious limited
- By the effects of the cascaded linear stages
- By the effects of the cascaded converters

Role of Architecture: Sigma-Delta Converters

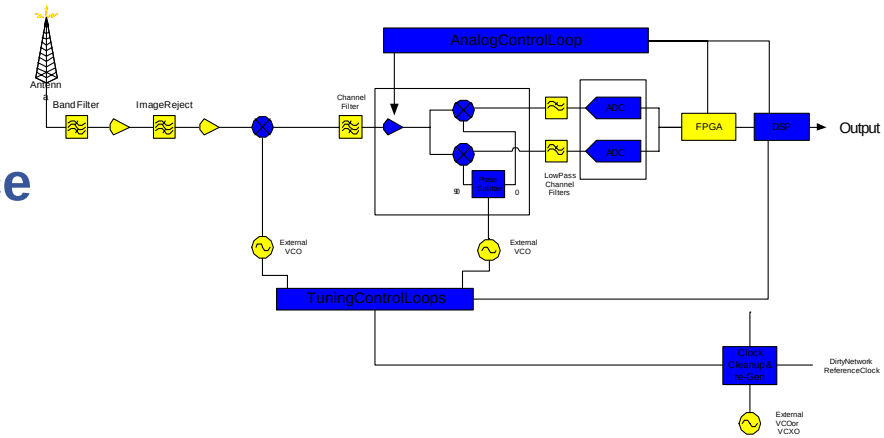


Really good for high resolution (20+ bits)
Really good for low to medium bandwidths (MHz)
Generally small chip area and ideal for integration
Baseband applications
Bandpass applications using down conversion techniques

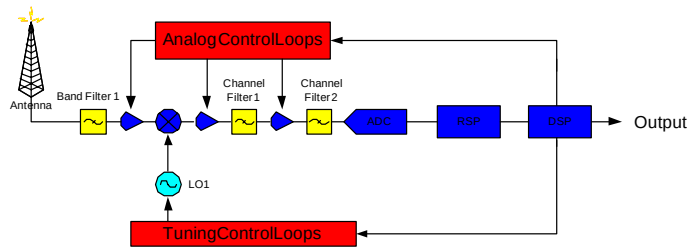
Limited sampling BW
- **BW proportional to clock rate and core ADC/DAC size**
  - Clock rate limited by process
  - Higher clocks mean higher power
  - Larger ADC/DAC size is more complexity and power
- **BW inversely proportional to decimation**
  - Decimation rate determined by ADC/DAC bits, clock rate and BW

Role of Application

- **Baseband Sampling**
  - Good Low frequency performance
  - Good 1/f characteristics
  - Good DC linearity

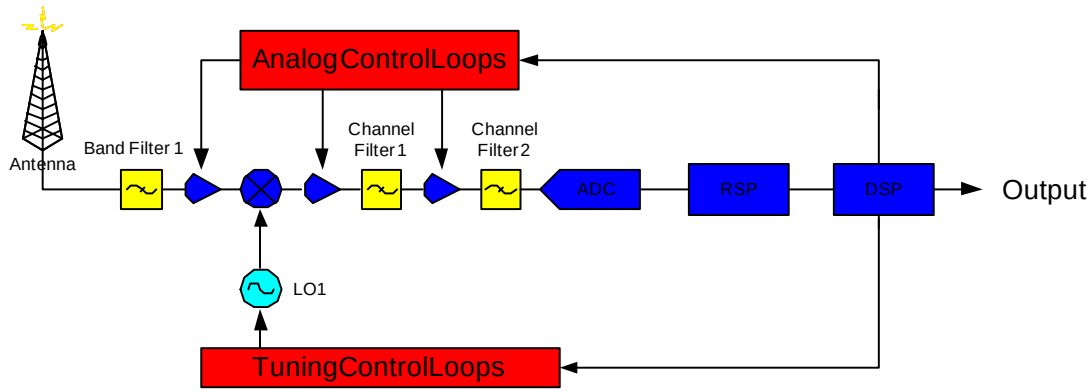


- **IF Sampling**
  - Good High frequency performance
  - Low aperture jitter
  - Good AC linearity
  - Higher Bandwidths



Role of Application

- **Single Carrier**
  - **Adequate Analog filtering makes digitizing easier**
- **Multi-Carrier**
  - **Wideband ADC input makes digitizing more difficult**



Communicating your needs

- **Digging out the true requirements**
- **Attaining Required Performance**

Understand Performance Requirements and budget in the ADC

- **Consider the ADC as part of the signal chain**
  - **Don’t look at noise and IMD for the analog front end and then add the ADC**
  - **Look at the system for small signal and large signal conditions performing sweeps where possible.**
- **ADC performance is different than other linear blocks**
  - **Noise is not white, it tends to be spotty.**
    - SNR is found by integrating the noise across the spectrum
      - Some parts of the spectrum will have better and worse noise than others
      - It changes with input drive level and frequency
  - **Spurious do not follow linear predictions based on order**
    - The transfer function can cause non-linear behavior performance variation
- **Model your scenario**
  - **Using accurate ADC behavioral models in system simulations can alleviate these uncertainties.**

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