HYPRES, Inc. Elmsford, NY

HYPRES Technology

HYPRES SME technology is
so accurate that it defines the Volt,
so sensitive that it measures brain currents,
so fast that it directly converts RF signals.

Based on a naturally occurring periodic quantum effect
— Rapid Single Flux Quantum (RSFQ)

Brings the Power of Digital Processing to the RF Domain and changes the Paradigm of Wireless Communications

SME = Superconductor Micro-Electronics

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Unique Features of Superconductor Technology

- **Ultra-High digital logic speed**

  Single Flux Quantum (SFQ) logic is the world's fastest
  (Devices ~10X faster than semiconductor, LSI ~ 50X faster than semiconductor)

- **Ultra-Low power dissipation**

  10,000X lower than semiconductor technology
  (Power dissipation for LSIC ~ 1 mW, Switching energy ~ 10^{-18} J)

- **Quantum accuracy**

  Defines the Volt
  (5ppb accuracy at 10V)

- **Fundamental linearity using magnetic flux quantization**

  Very High-SFDR ADC and DAC
  (Conversion between analog and digital domains through flux quantum (Φ_0 = h/2e) is independent of circuit parameters)

- **Extremely high sensitivity**

  SQUID (ADC front-end) is <u>the</u> most sensitive energy detector
  ~60dB better than conventional semiconductor front end (Example ~ -155dBm for 1 MHz BW, with slope of 20 dBm/decade)

- **Extremely low noise**

  Receiver System Noise Temperature T_S ~ T_A
  (Thermal noise is essentially "0")

- **Ideal interconnects**

  Speed-of-light transmission in LSI circuits, no RC delay
  Low-impedance superconductor interconnects have negligible loss, dispersion and crosstalk

- **Simple, inexpensive IC fabrication**

  Much less expensive complex chips and facilities/equipment to produce chips than semiconductors
  (~10 steps, no expensive operations, Thin Film)

Result: Digital-RF Technology

High-fidelity, wideband, high-sensitivity digital representation and subsequent processing ("RF DSP": channelization/correlation, spectrum control, broadband beamforming,..) of RF waveforms

Market Applications

- **Wireless Communication**
  - **Mobile and Fixed Cellular**
  - **Satellite**
  - **Terrestrial**
  - **Switches and Routers**

  (Military, Commercial, & Civil)

- **Additional Markets**
  - **Defense — EW, SIGINT, RADAR, …**
  - **Ultra-High Speed Computing**
  - **Instrumentation**
  - **Medical**

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Commercial Wireless Base Stations

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HYPRES Product Benefits for Wireless Networks

Summary

- Massively Reduced Network Capital Expenditures
  - Much Fewer Base Stations
  - Lower Capitalization per Base Station
  - Postponement ("one size fits all"– "air interface immune")
- Substantially Reduced Operating Expense
- Enhanced Revenues and Margins
- Significantly Enhanced Performance
- Unparalleled Reliability & Flexibility
- A "Natural" for Distributed Radio (over fiber, etc.)
- Boost Spectral Efficiency (HSDPA, etc.)
- Future-Proof Products -- beyond 3G (>30Mb/s inherent)
- Extended Mobile Battery Life/Throughput

HYPRES Digital-RF enables the next generation Base Station

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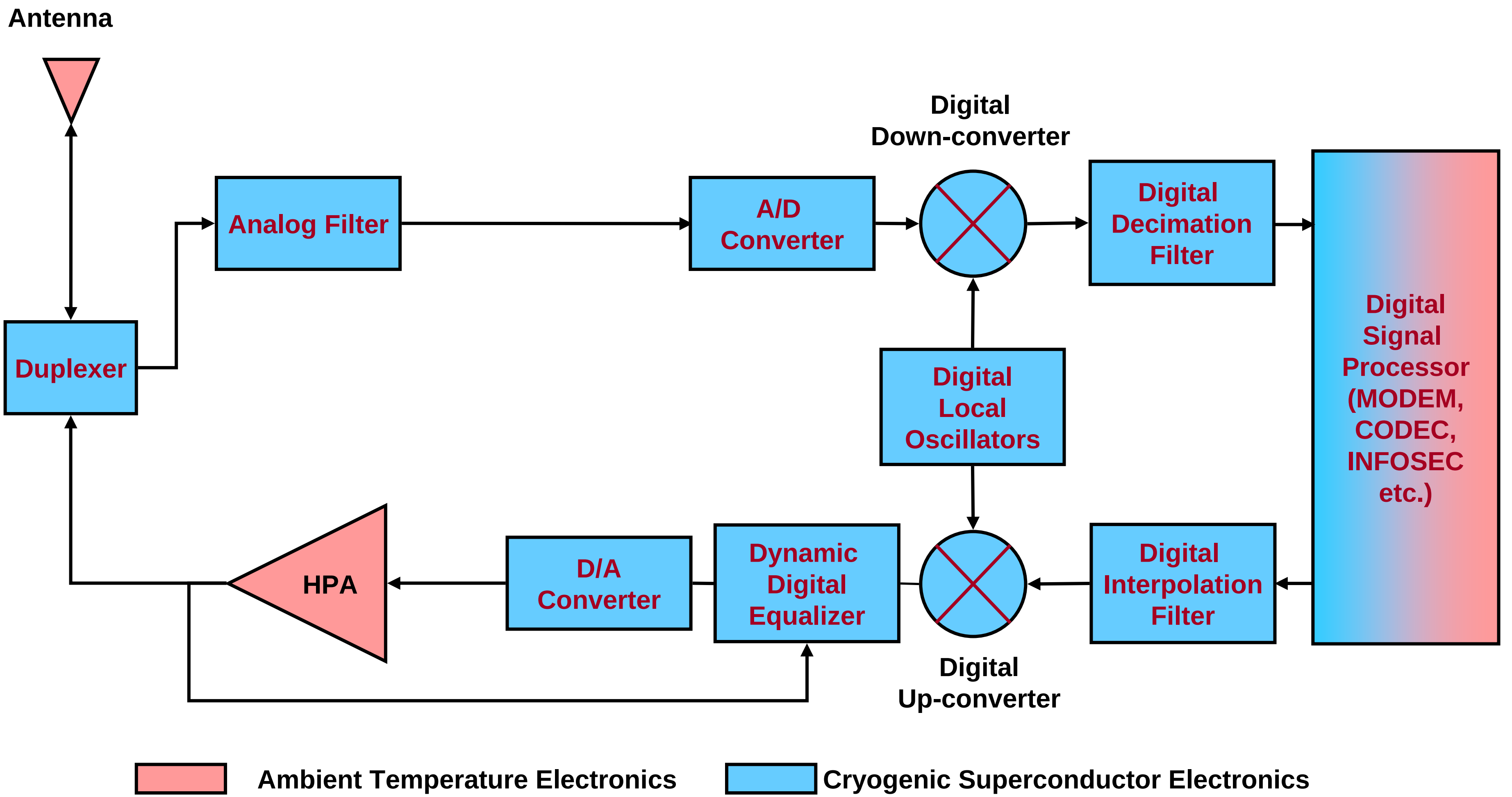
Digital-RF Transceiver



Brings the power of digital processing to the RF domain

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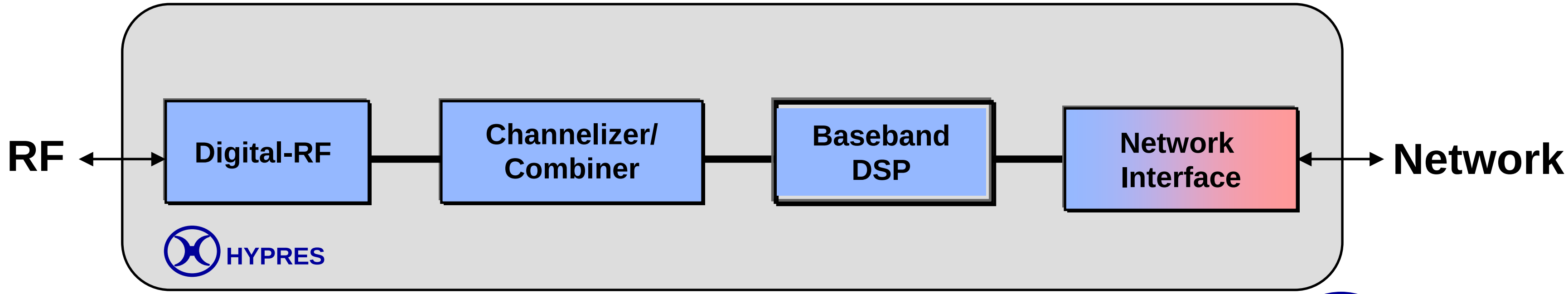
Complete Digital-RF Transceiver

Enables the All-Digital Software Radio

Commercial Version

☐ Total functionality of a base station in a single product

excluding power amplifiers, antenna/tower, and standard ancillary equipment



Cryogenic Superconductor Electronics | Ambient Temperature Electronics

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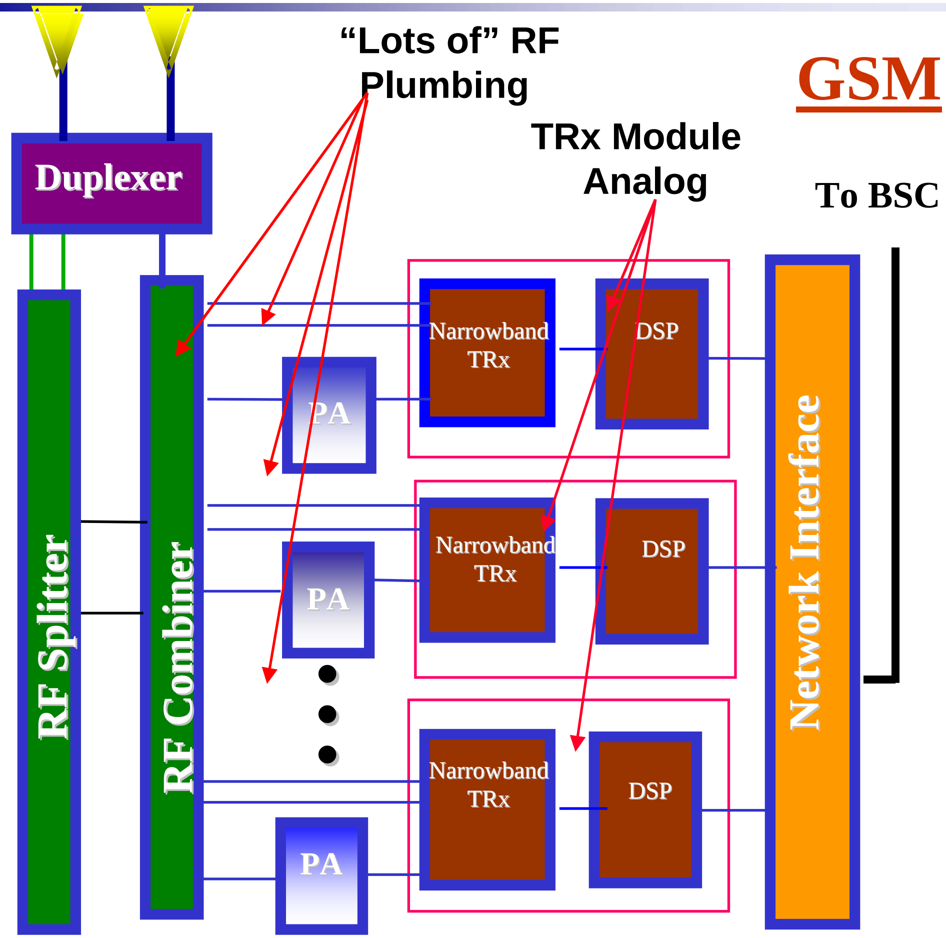
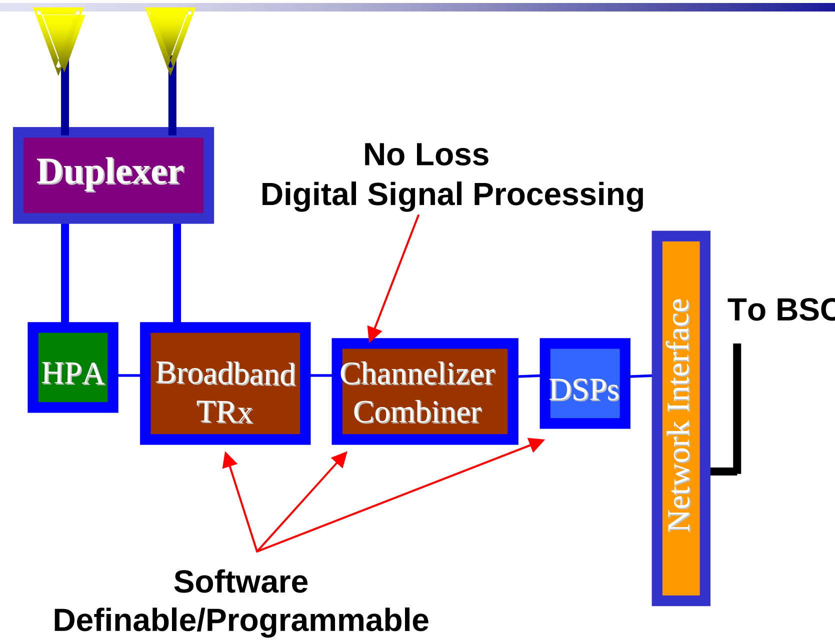
Traditional Base Station Electronics vs. HYPRES Base Station Electronics





Ultra Wideband for HYPRES SME

- Multi-Protocol "Future Proof"
- Software Definable, High Speed Data Ready
- Loss Free, Digital RF Combining/Splitting
- Least Hardware, Highest Reliability, Lowest Cost

- Expensive
- Difficult to upgrade and add channels
- Inefficient – multiple transceivers
- Inefficient – multiple PA and lossy combiners
- Very inefficient for high speed data
- Bandwidth limited

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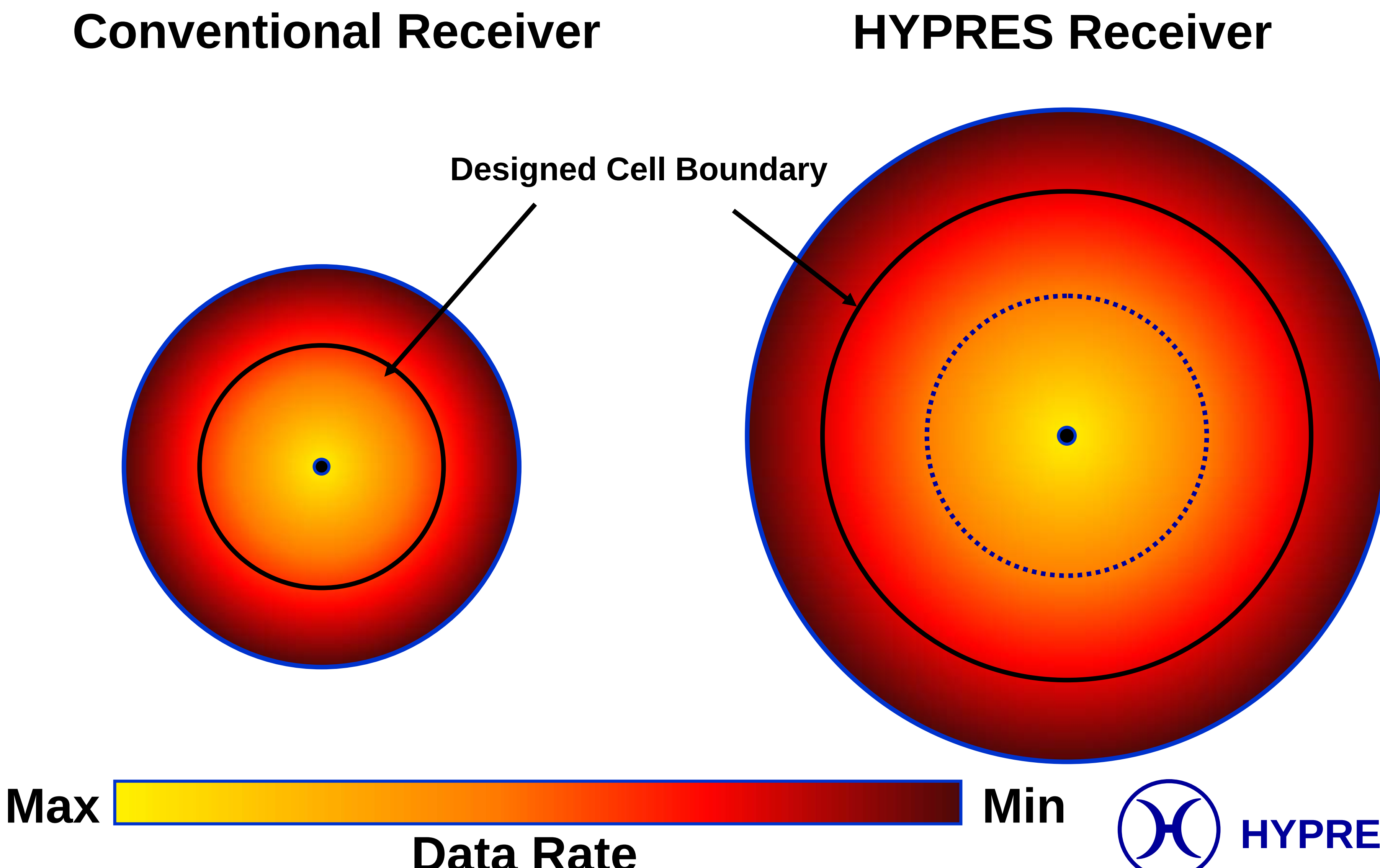
Expanded Range of High Maximum Data Rate



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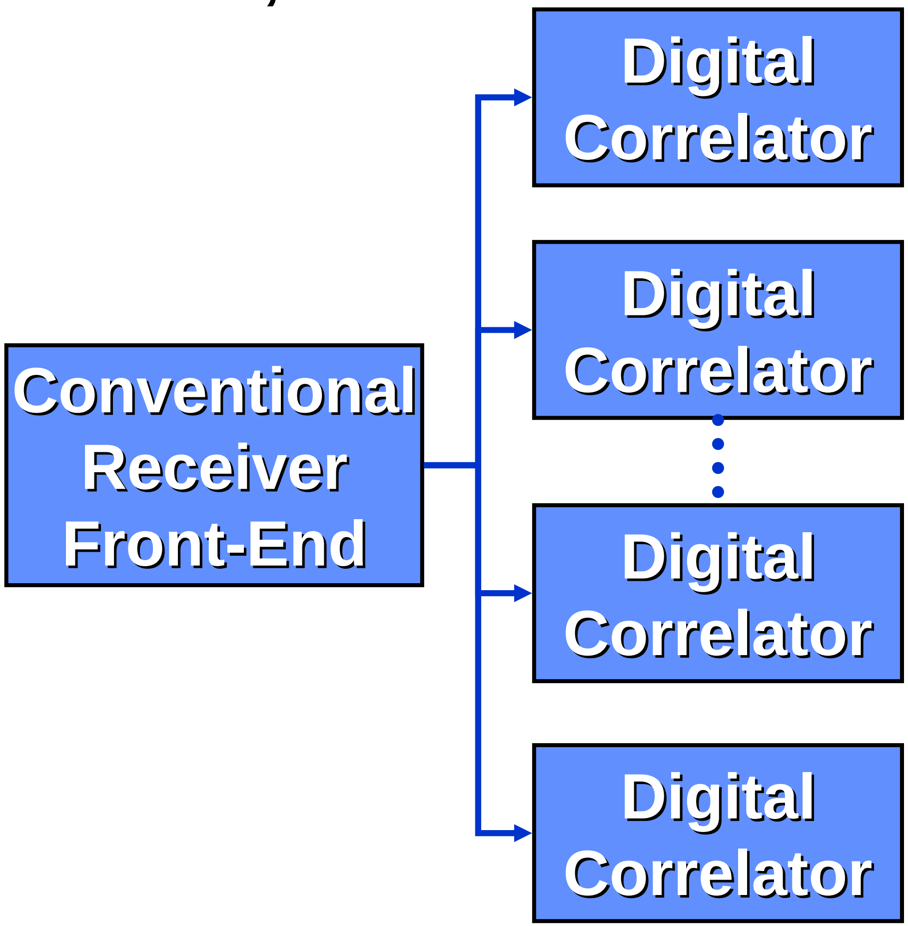
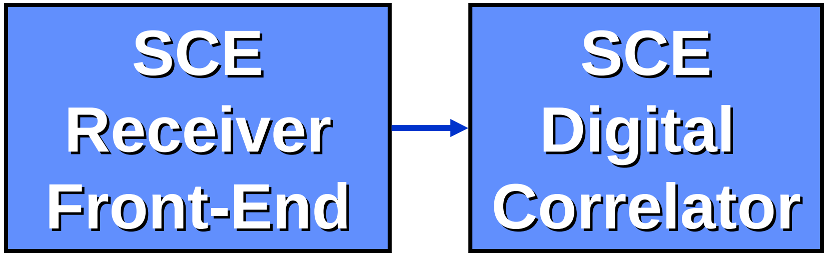
Massively Time-multiplexed Processing

- Conventional Processing
- Slow, Parallel Hardware



- HYPRES SME Processing
- Fast, Serial Hardware
  - Time-sharing of tasks
  - Hardware re-use
  - Uniquely flexible

Major Cost Saving



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Multi-User Detection (MUD) for UMTS & CDMA

- CDMA systems are severely interference limited

SNR = S/(N+I), N<<I

- Removing interference through multi-user detector can **increase system capacity by 2-10X**
  - This also enables higher data rates, low mobile power, and easier system administration
- **Successive Interference Canceller (SIC)** is a multi-user detector scheme for removal of interferers in sequential steps of interference estimation and subtraction
- Sequential subtraction provides better interference cancellation at the expense of greater processing

Tera-Operations DSP Required

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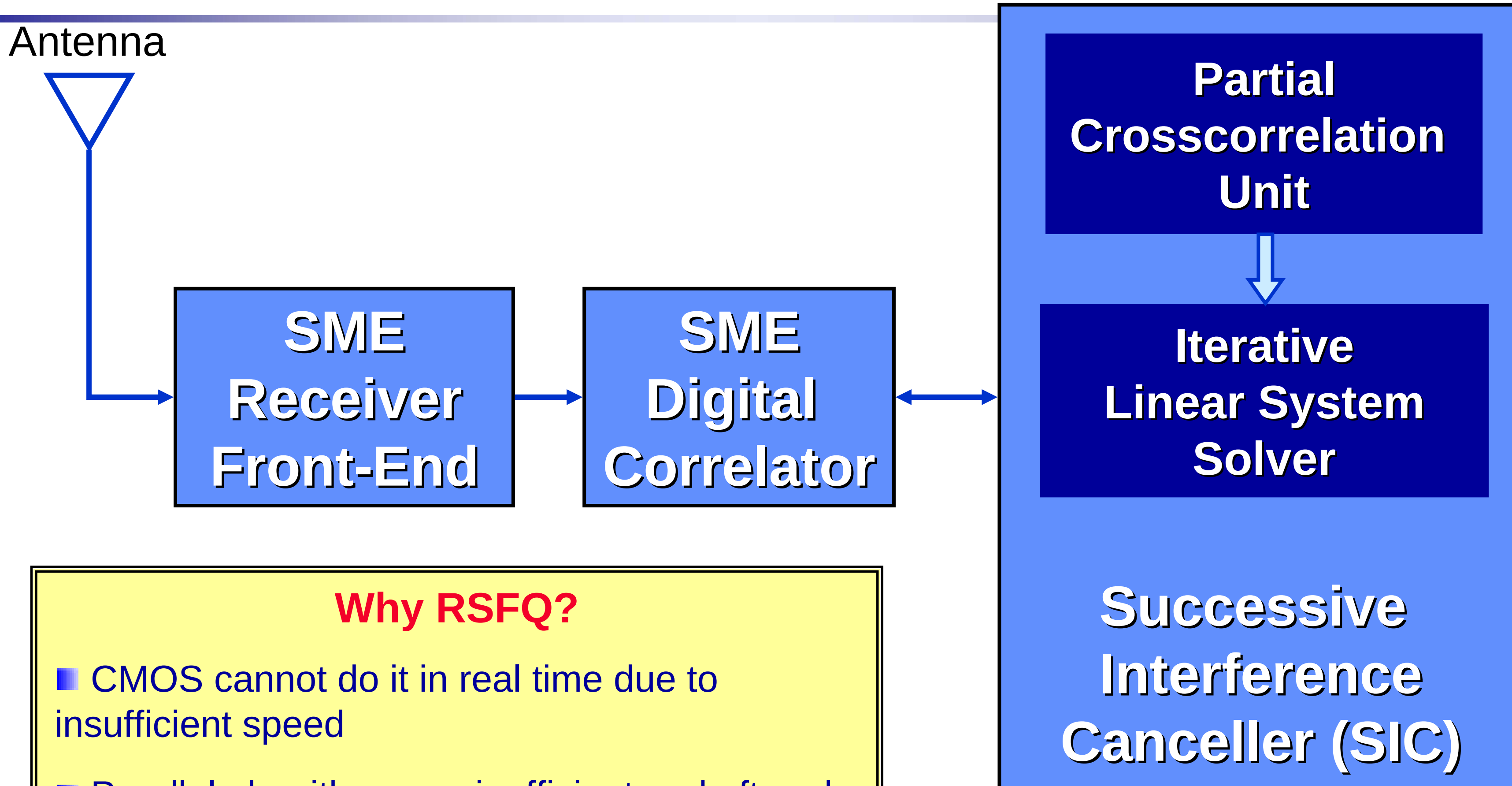
RSFQ Successive Interference Canceller



Why RSFQ?

- CMOS cannot do it in real time due to insufficient speed
- Parallel algorithms are inefficient and often do not converge at all
- RSFQ SIC is based on a simple Gauss-Seidel iterative algorithm that converges quickly

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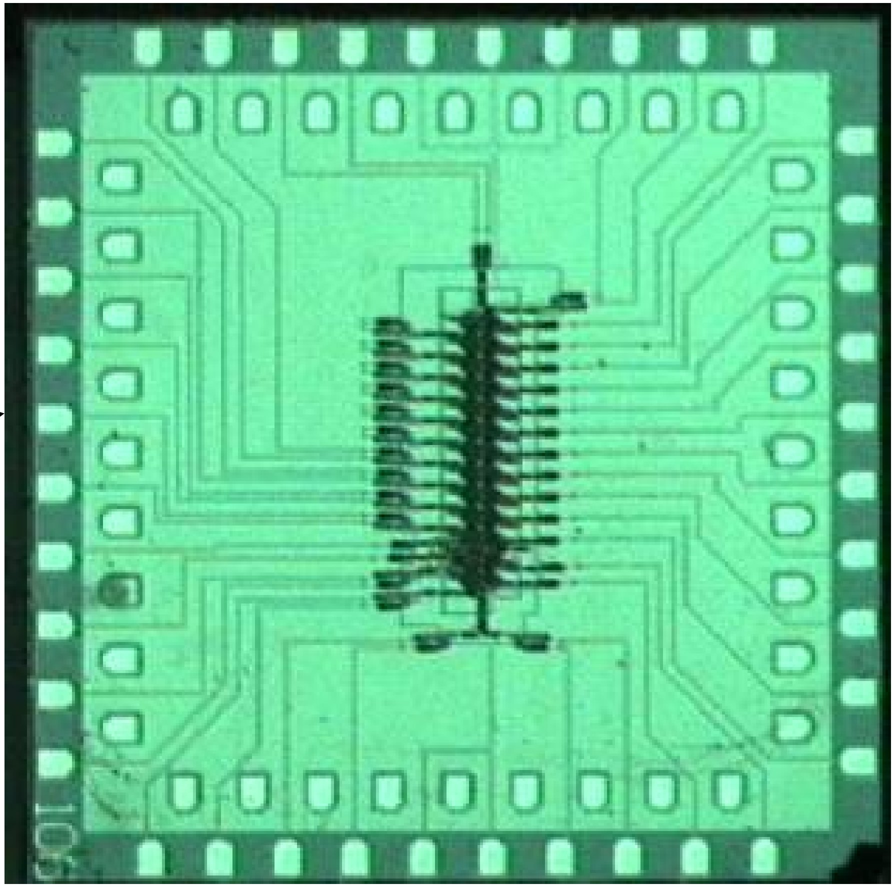
Prototype SIC chip

Spreading Code Generator
&
Multiply Accumulate Unit



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Superconducting Back-End Processors

- **Superior speed of SME can produce independent multi-Tera-Ops back-end digital signal processor products for conventional transceivers**
  - **Successive Interference Canceller (SIC) to sequentially cancel interferers, starting with the largest one -- Large (up to ~ 10X) increase in capacity**
  - **Massively time-multiplexed correlation-based Walsh-Hadamard (WH) Demodulator -- Large cost savings**
    - Separate WH Demodulators are now used for each multipath of each reverse link being processed by a base station (parallel processing)
    - Serialization of tasks using SME processors provide hardware savings by more than an order of magnitude (serial processing)

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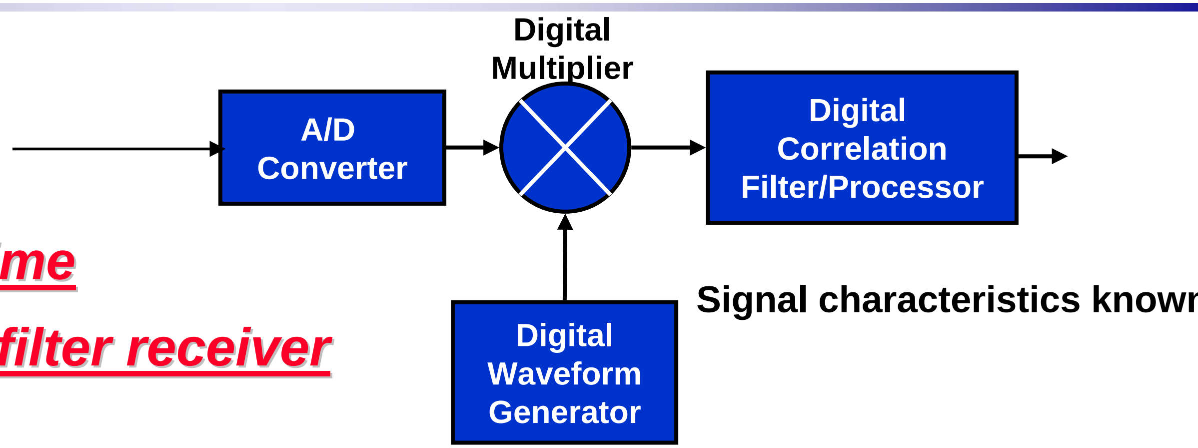
HYPRES SME Correlation-Based Receivers Provide Optimum Performance in the Digital-RF Domain



In near real time

the optimum matched filter receiver

- **Uses matched waveform to perform digital filtering (correlation) in both the time and frequency domain achieving maximum receive efficiency**
- **Hardware is not specific to any analog/digital modulation (FM, PM, MPSK, etc.) or multiple access scheme (FDMA, TDMA, CDMA, MIMO, OFDM, etc.)**
- **Real-time Correlator combines functions of downconversion, demodulation, and decoding ⇨ Direct RF Digital Demodulation in one unit**
- **Rapid Φ locking to RF carrier permits tracking of signals with time varying phase and frequency: Tx drift, Doppler-shift, signal hopping, etc.**
- **Processes out (suppresses) un-correlated noise & interference over repetitive samples; i.e., increases the system SNR & SIR**

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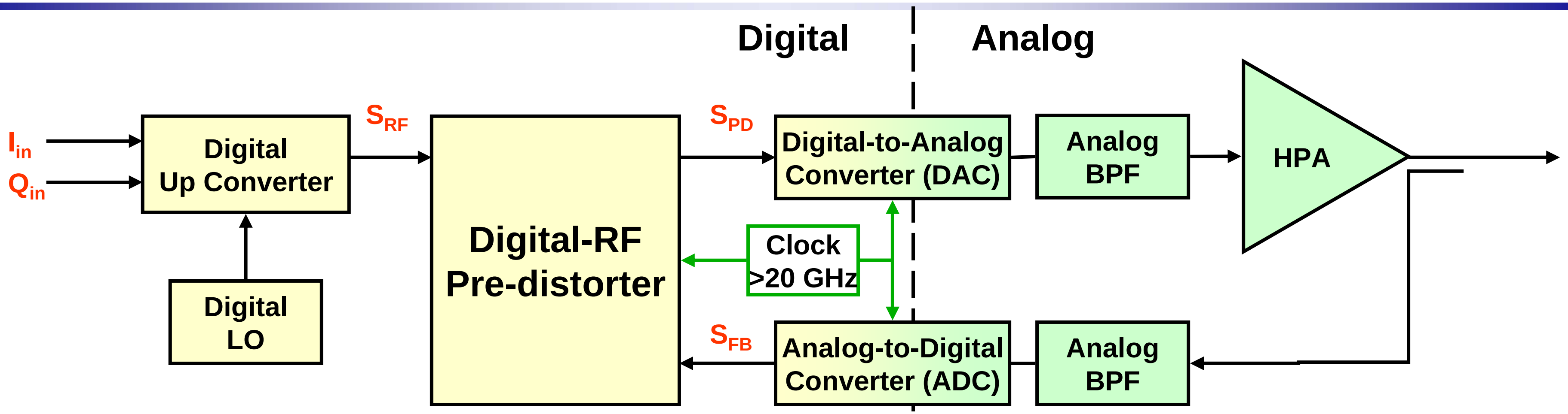
Power Amplifier Linearization

[Multi-Carrier Power Amplifiers]



- Near real-time true digital Adaptive Linearization ***at RF***
- Far better than
  - Digital baseband predistorters (Enhanced Efficiency)
  - Feed-forward amplifiers (Lower Distortion)
- Frequency (& Data Rate) independent from 25% to 50% Clock Rate
- Efficiency enhancement up to the inherent limit of the HPA
  - Allows use of lower cost HPA

One HPA Covers Ultra-Wide Bandwidths Consuming Far Less Power

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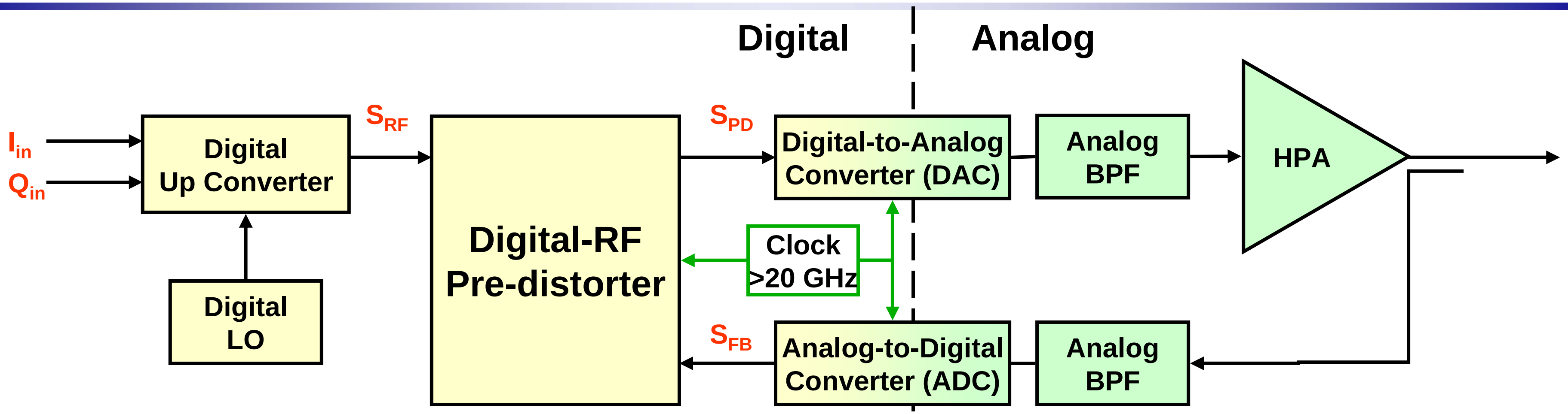
Power Amplifier Linearization
[Multi-Carrier Power Amplifiers] (continued)



- **Full bandwidth for all air interfaces (waveforms)**
  - For example, 60 MHz for UMTS (limited only by PA bandwidth)
  - Adjust power in each band for traffic matching in near real time vs inflexible passive combining of multiple PAs
- **Dramatic reduction in overall power consumption***
  - "Iceberg effect" = smaller & lower cost: A/C, power supply, UPS / UPS batteries, cabinet, cooling, and
- **Allows use of lower cost HPA**

Huge reduction in PA and ancillary equipment COST

One HPA Covers Ultra-Wide Bandwidths Consuming Far Less Power

* Increase of efficiency from 25 to 50% or 75% reduces power dissipation by 66.6% to 90%

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Adaptive Antennas

Digital-RF

Beamforming & Nulling

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Digital-RF Beamforming

- Beam directions defined by setting appropriate true time delays, corresponding to a wavefront
  - Set coarse digital delay between antennas by cross-correlation with discrete steps of 25 ps
  - Tune digitally controlled analog (continuous) delays for each antenna by interpolation to <1ps
- Beam directions are the same for receive and transmit due true time delay phasing
- Enables multiple beams and adaptive nulling
  - Significantly augments AJ, LPI, LPD & LPE
  - Further suppression of interference

Note: 1ps is < 1 degree at 2GHz

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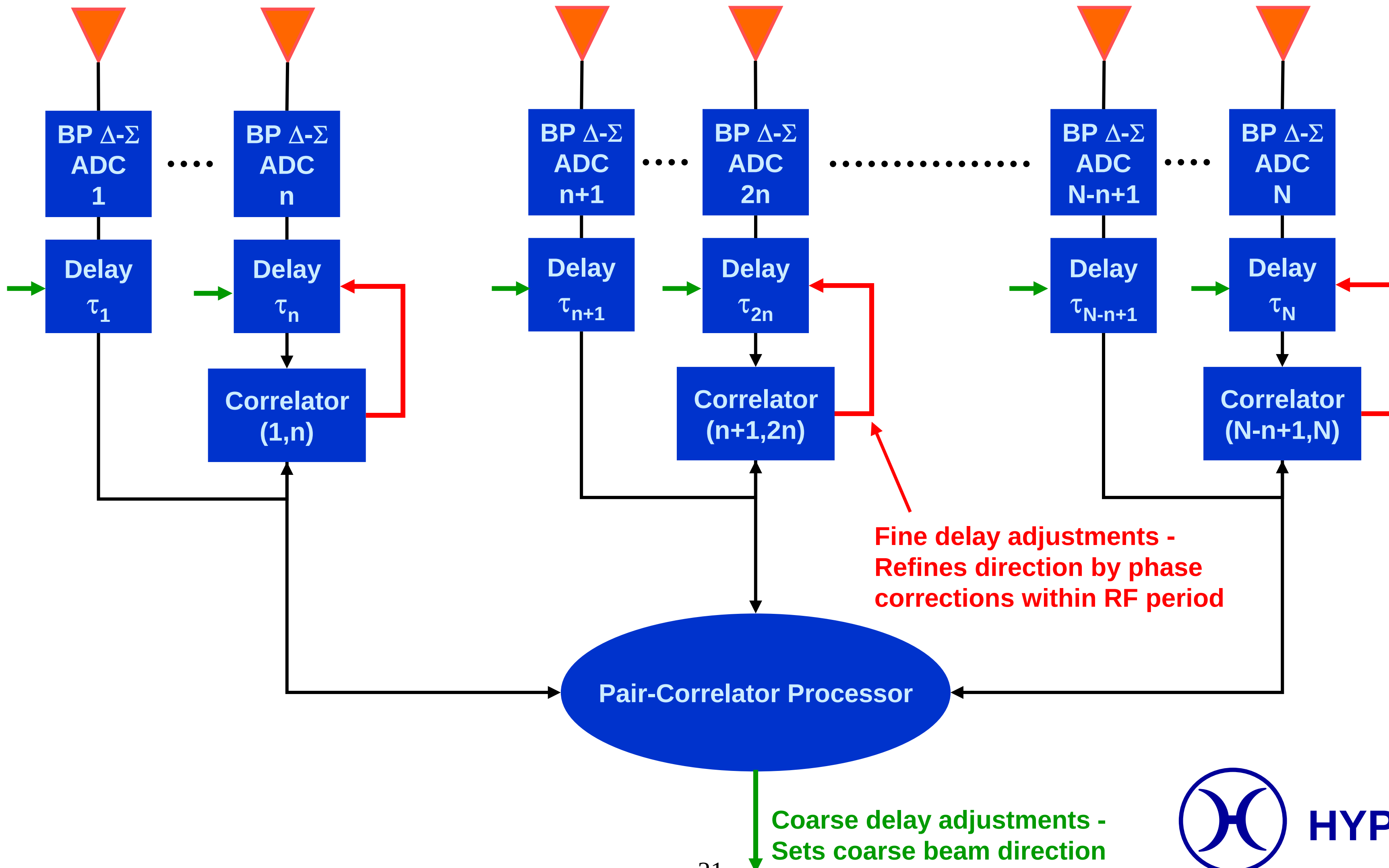
Coarse Delay Adjustments for Arraying



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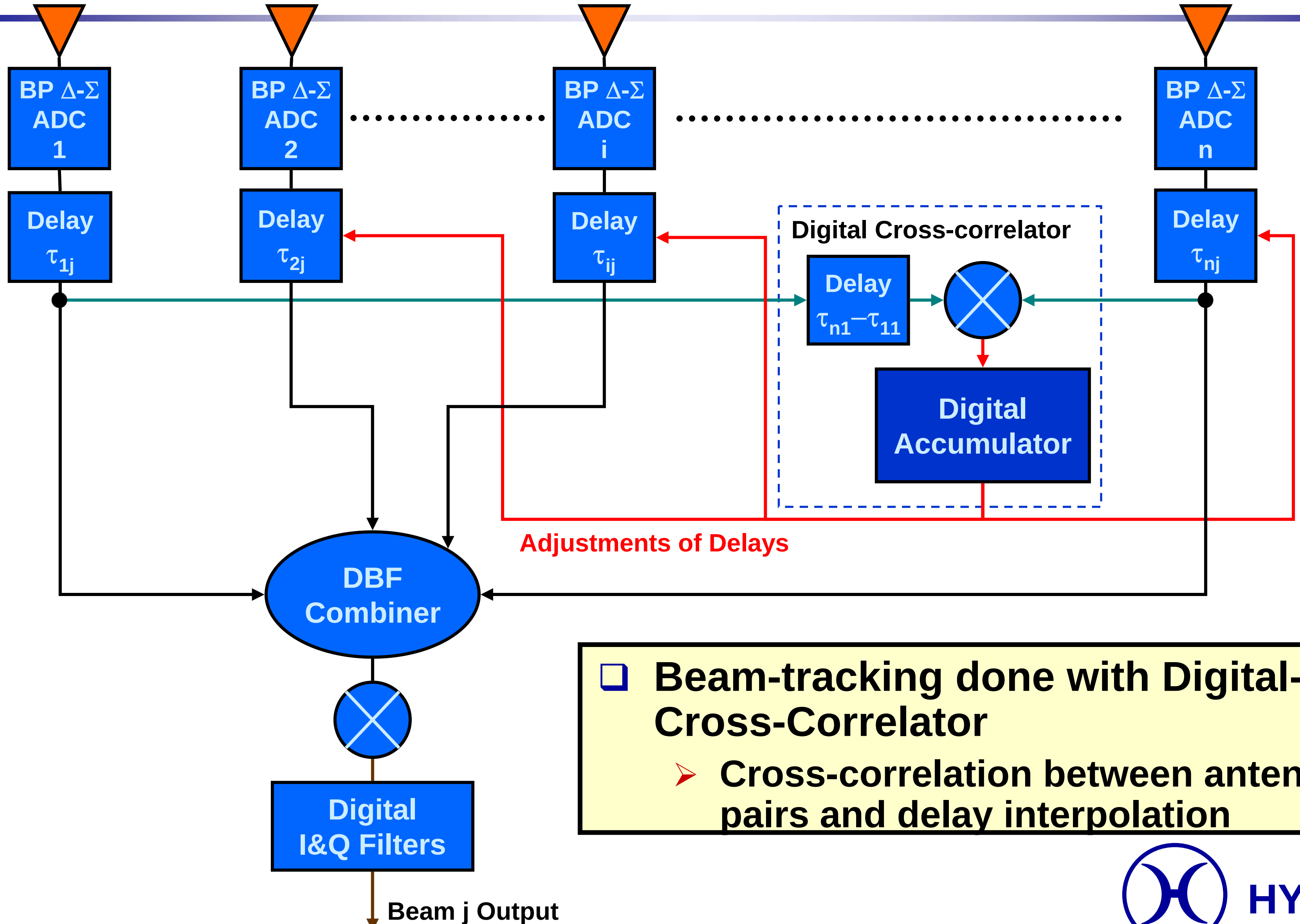
Fine True Time Delay Adjustment



- Beam-tracking done with Digital-RF Cross-Correlator
  - Cross-correlation between antenna-pairs and delay interpolation

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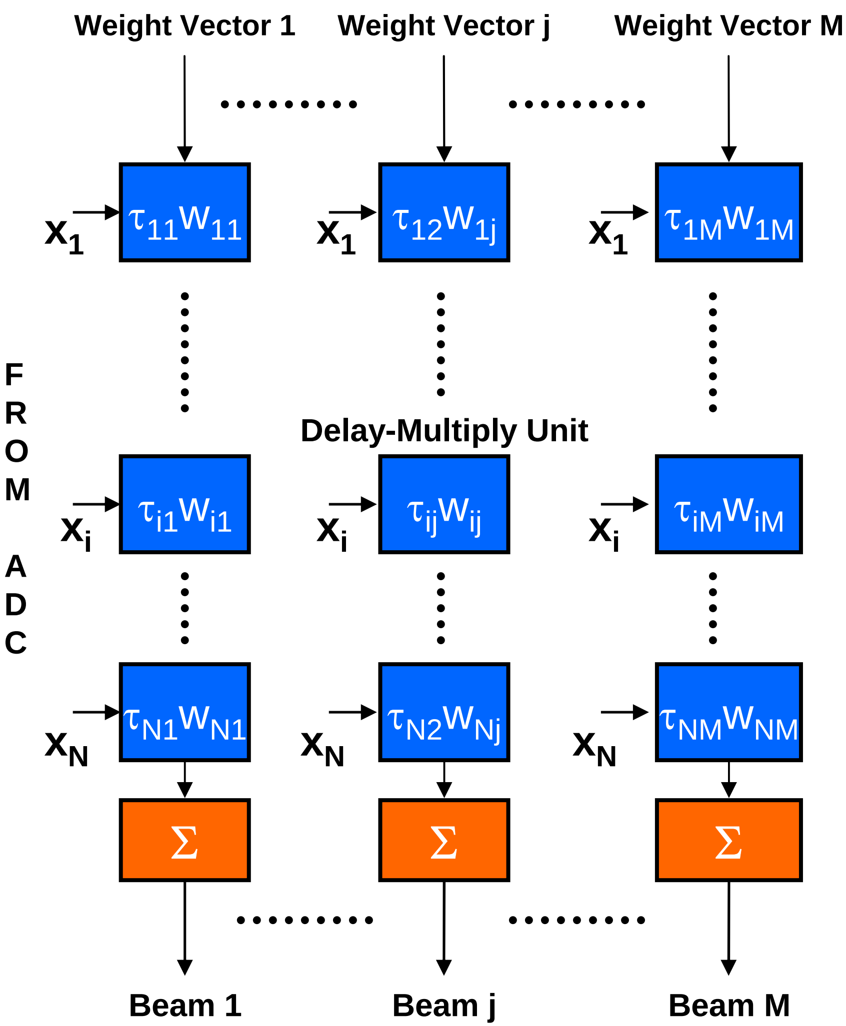
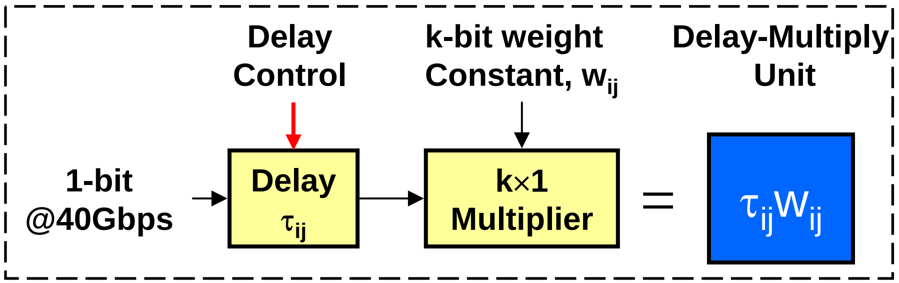
Adaptive Digital-RF Beamforming





$$Y_j = \sum_{i=1}^{N} X\left(t - \tau_{ij}\right) \cdot W_{ij}$$

Output of each antenna:

- Digitized at RF
- Split into M digital copies for M beams
- Each copy delayed by TTD (τ_{ij})
- Multiplied by Weights (W_{ij})
- Summed to form each of M beams

The Ultimate in Diversity

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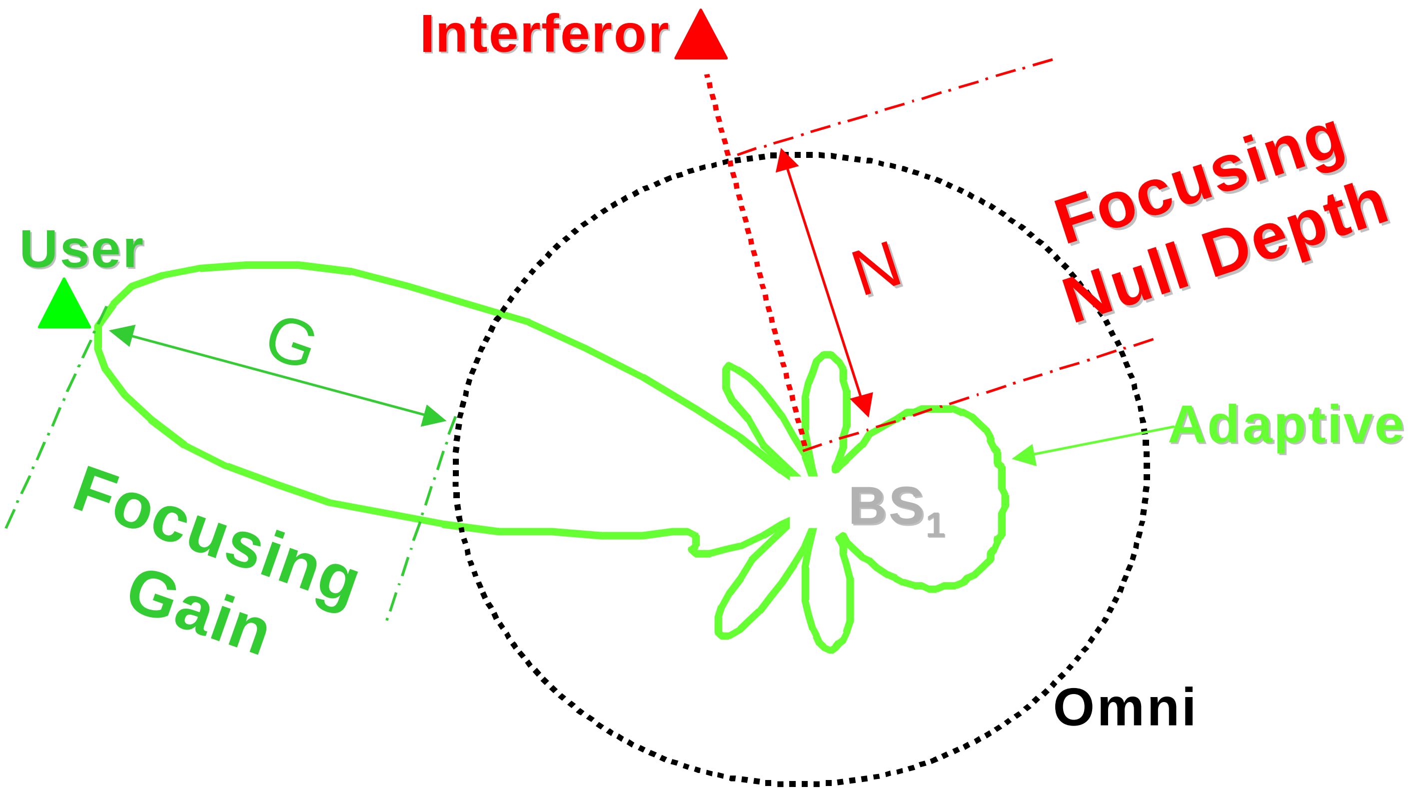
Directive Gain and Nulling Increase C/I



Adaptive Processing Gain = G + N

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Adaptive Array Processing

- Reduced phase error provides deeper nulls, better C/I :
  - **Phase error using active nulling:**
    - 5 degrees of phase error allows deepest null of -27 dB
    - 10 degrees of phase error allows deepest null of -21 dB
    - 20 degrees of phase error allows deepest null of -15 dB
- Reduced amplitude error provides deeper nulls, better C/I:
  - **Amplitude error using active nulling:**
    - 0.25 dB of amplitude error allows deepest null of -25 dB
    - 0.5 dB of amplitude error allows deepest null of -19 dB
    - 1.0 dB of amplitude error allows deepest null of -13 dB

Digital-RF technology produces ultra-broadband 60 dB nulls:

< 0.1 degree in phase

< 0.01 dB in amplitude

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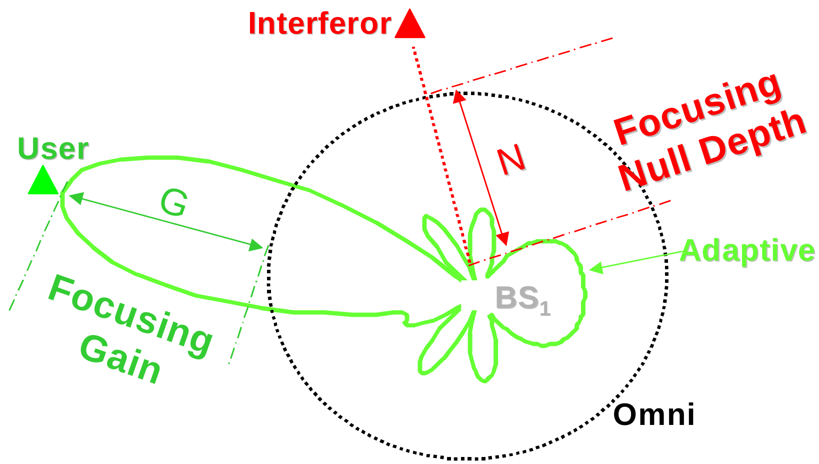
Increasing C/I -- Reverse & Forward Links



Adaptive Processing Gain = G + N

HYPRES Digital RF technology
- **Produces 60 dB nulls**
- **Full Gain**
- **On Receive and Transmit**

It is better to increase N (nulling) than increase G (antenna gain)

Increasing G requires larger antennas

- Need to effectively double the size for (only) a 3 dB increase
- More expensive, higher tower loads, environmental restrictions

Increasing N requires finer and more stable amplitude and phase

- Offers the potential for smaller antennas
- Less expensive, lower tower loads, and less environmental issues

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HYPRES Digital-RF -- Adaptive Antennas(++)

- **Makes virtually any antenna set into adaptive arrays**
  - Big, ugly, and expensive → small, elegant, and cheap
- **Significantly improves the C/I by (very) many dBs**
  - Base Stations & Mobiles
  - Much better than other alternatives (frequency hopping, AMR, etc.), but can be combined with these other alternatives for added improvements
  - Spatial Diversity –minimizes fading and effects of multipath propagation, and reduces the effective delay spread of the channel, allowing higher bit rates to be supported.
- **Balances the forward and reverse links**
- **+ Adaptive Sub-Sectorization -- ultimate in performance**
  - Ultra-dynamic control to match traffic density conditions in near real time

Enables HUGE increases in Range/Capacity/Flexibility for GSM, CDMA, GPRS, EDGE, UMTS, and beyond

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MIMO -- Another Example

Multiple Input/Multiple Output (MIMO) requires very accurate time synchronization, and ability to discriminate/extract signals on the same frequency with the same code.

Digital-RF Correlator:

- Uses matched waveform to perform digital filtering (correlation) in both the time and frequency domain achieving maximum receive efficiency
- Rapid Φ locking to RF carrier permits tracking of signals varying in time, phase and frequency
- Suppresses un-correlated noise/interference over repetitive RF-rate samples
- HYPRES Multi-GHz clocks are ultra-stable [jitter measured in femtoseconds (10^{-15}s)]

Correlates UMTS user signals in same band and same code separated by only 6 inches

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MIMO -- Another Example
(continued)

Correlates UMTS user signals in same band and same code separated by only 6 inches

Adds new dimension -- Range Sectorization
A dramatic increase in capacity

Digital-RF offers an unprecedented and exceptionally cost-effective solution that has the potential to increase capacity on forward and reverse links by 10 X

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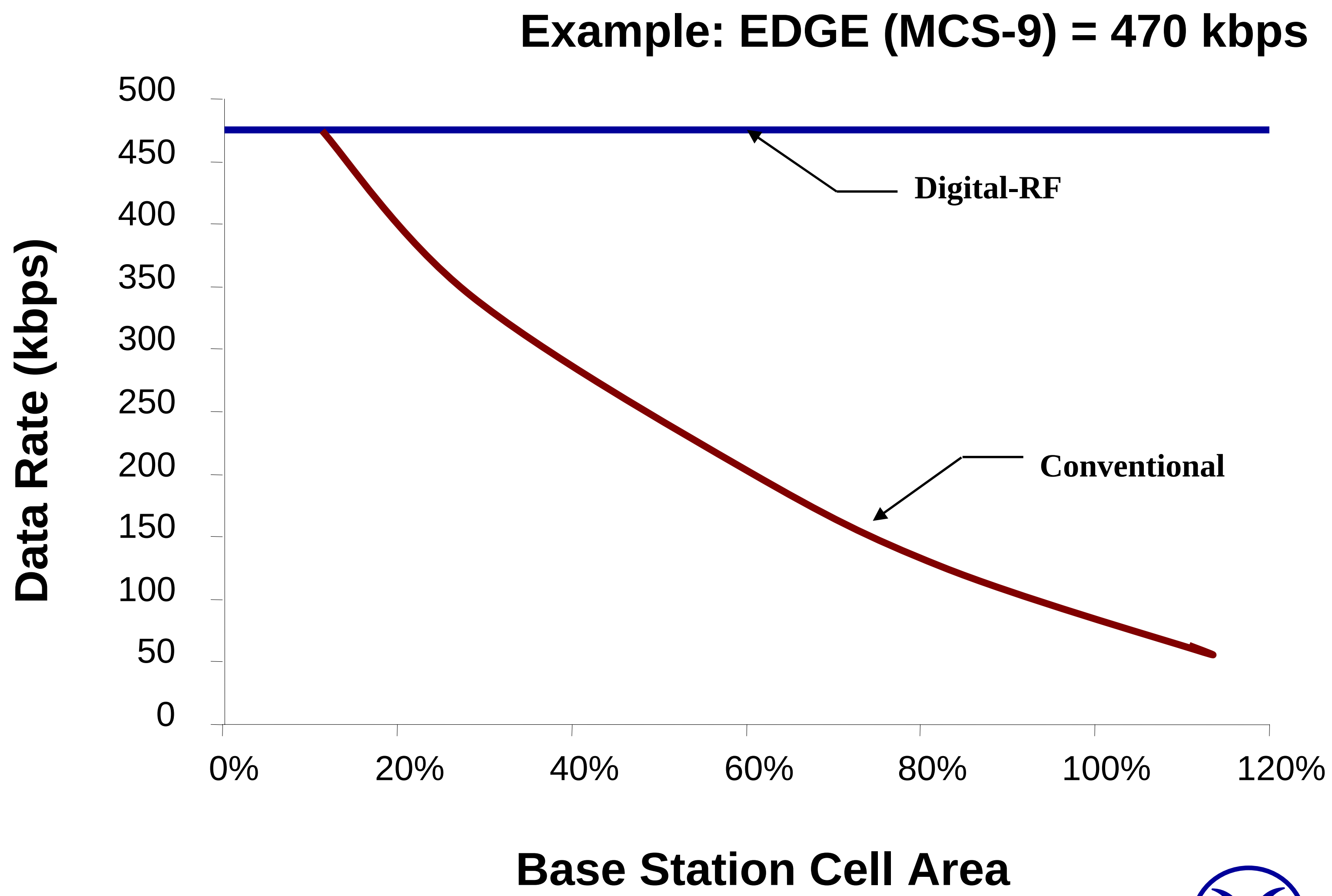
One Digital-RF Base Station

[versus 10 to 14 Conventional]



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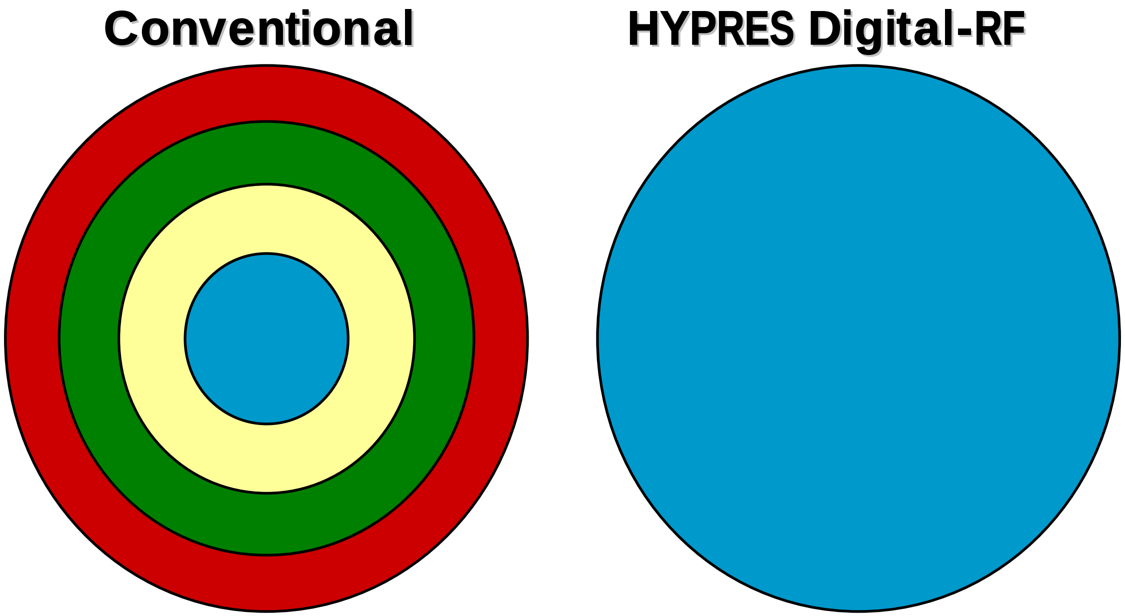
Digital-RF

Unparalleled Performance – Dynamically* Allocated Resources
[* measured in nanoseconds]

Peak Data Rate

- 70 kbps (MCS 1)
- 140 kbps (MCS 4)
- 240 kbps (MCS 6)
- 470 kbps (MCS 9)



Can dynamically adjust to traffic density, including “inverse breathing”
- Higher density for close-in “range cells” during the day
- Higher density for far-out “range cells” during the night

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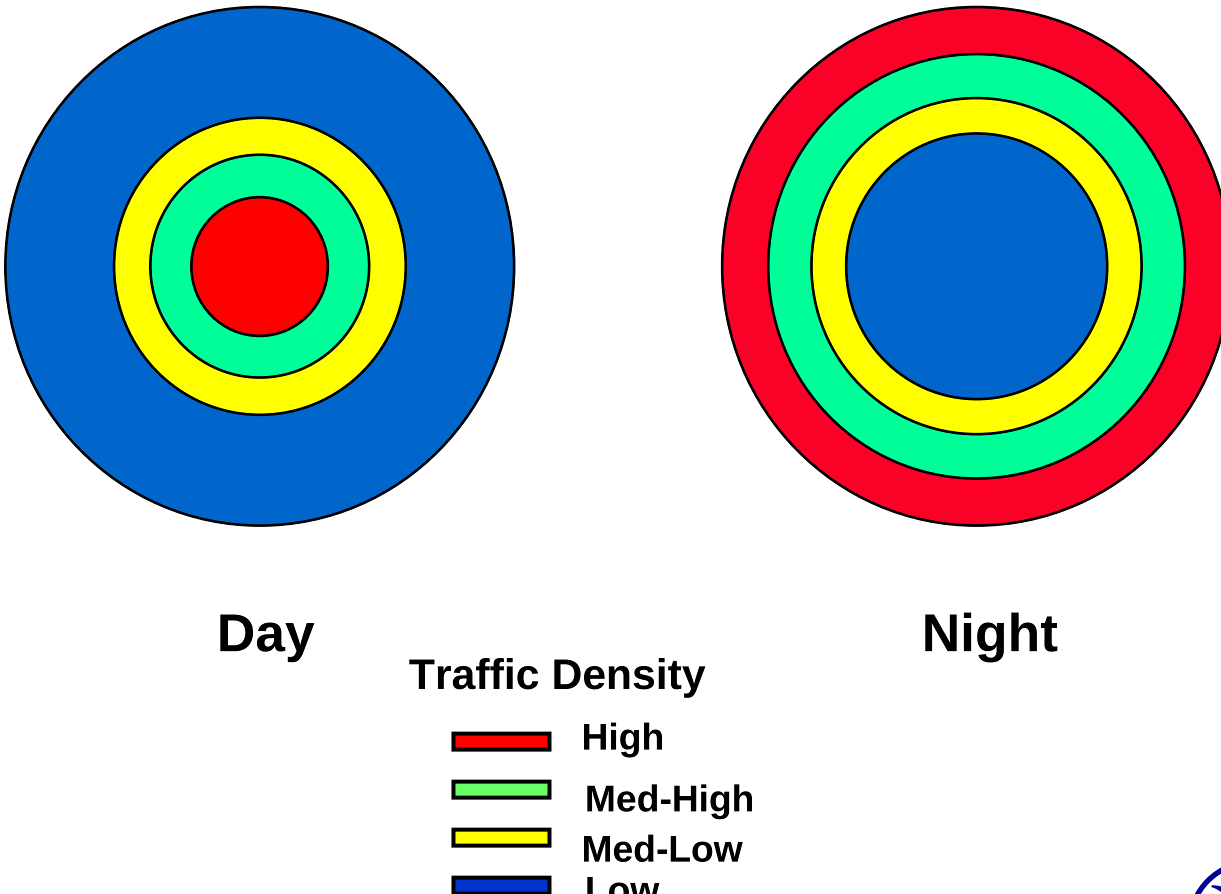
Inverse Breathing

Unparalleled Performance – Dynamically* Allocated Resources

[* measured in nanoseconds]



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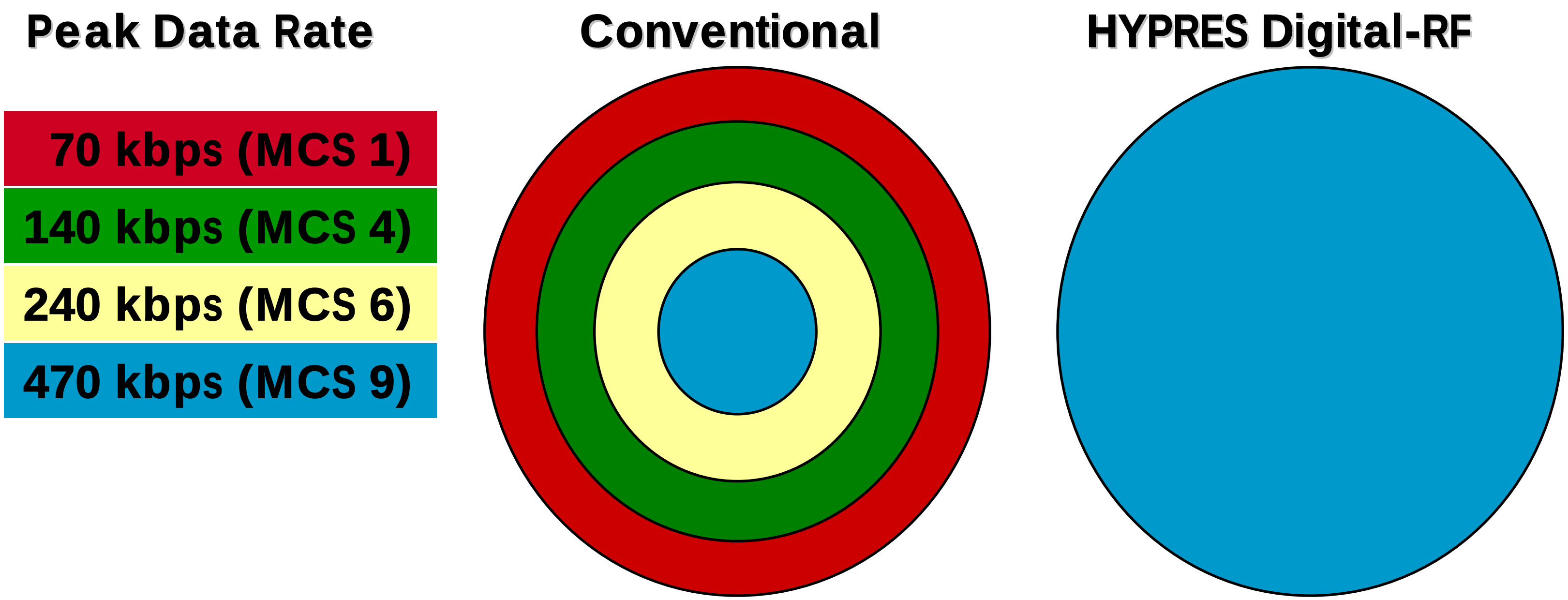
Some Additional Potential Benefits

- Reduce backhaul cost by using much higher capacity in-band channel and cross link to central sites
- For distributed radio and/or Remote RF head SME ultra-high speed I &Q channelization (prior to processing) is a natural for fiber or microwave connection



- **E911-** Ultra high sensitivity, range and range determination capability may provide an option to geo-locate using multiple towers w/o use of location devices in mobiles

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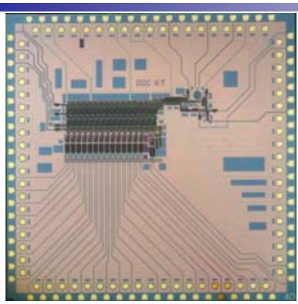
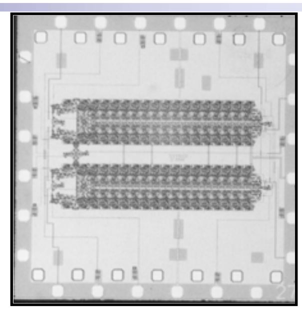
HYPRES Digital-RF Infrastructure

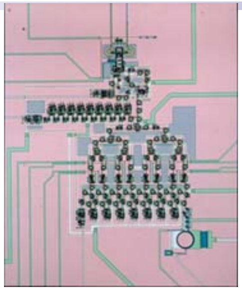
Fundamental Proof of Performance Established



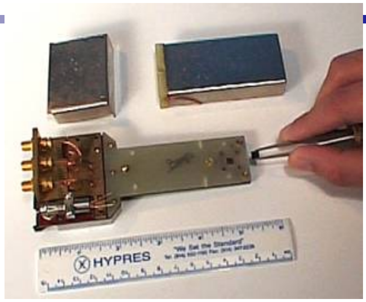
Analog-to-Digital Converter (ADC)



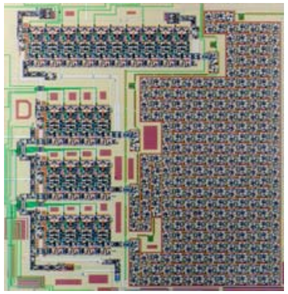
Multiplier



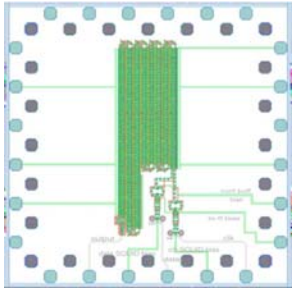
Low-jitter On-chip Clock



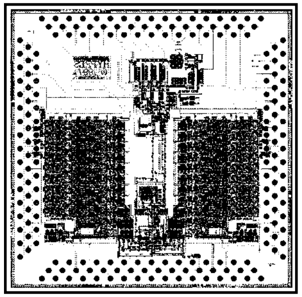
Optical I/O and Packaging



Digital-to-Analog Converter (DAC)

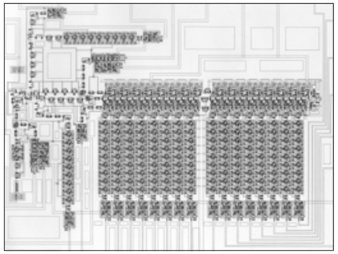


Shift Register



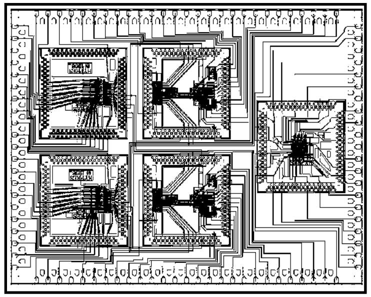
Digital I&Q Converters

User Interfaces

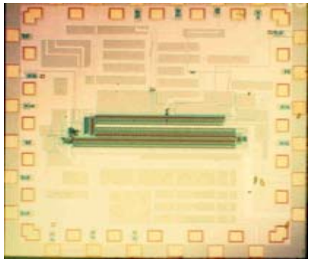


Correlator

Random Access Memory (RAM)



Multi-chip Module Packages (MCM)



Delay line

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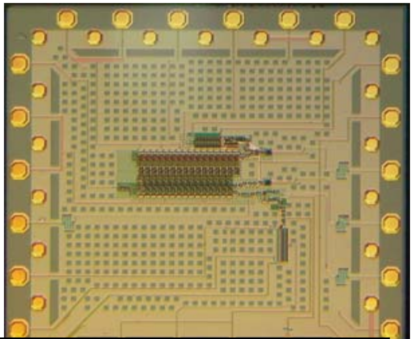
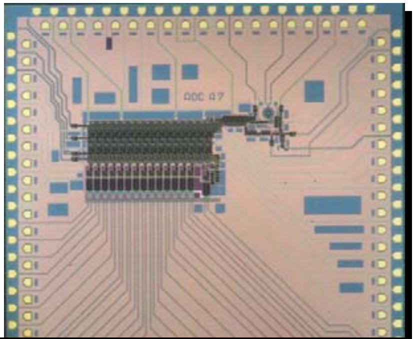
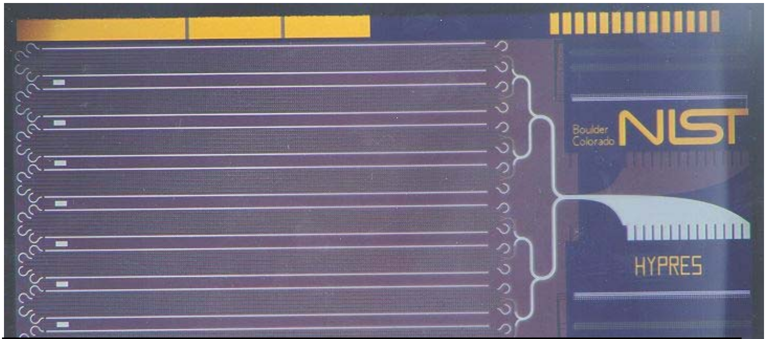
Low-temperature Superconductor (Nb) ICs



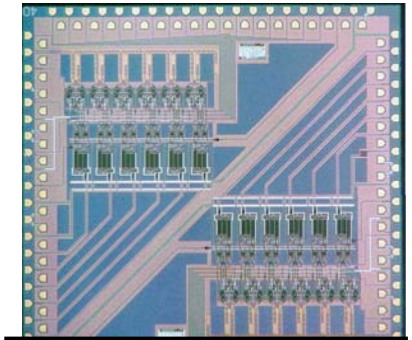
Time-to-digital Converter with on-chip 40 GHz clock



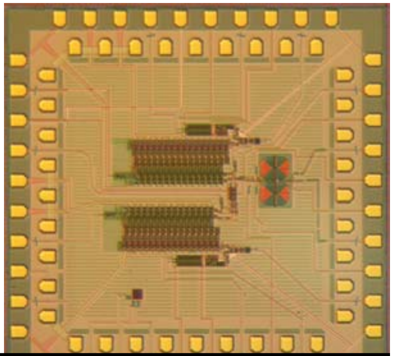
15-bit Analog-to-digital Converter with 20 GHz clock (98dB SFDR@ 10 MHz)



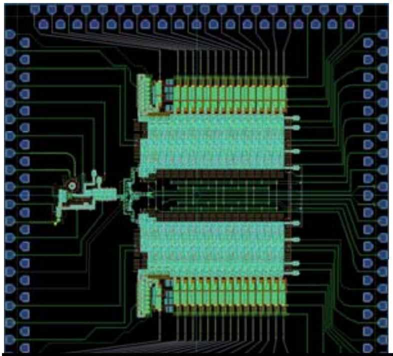
1cm x 2 cm 10 Volt Chip with 5ppb accuracy (>20,000 Josephson junctions)



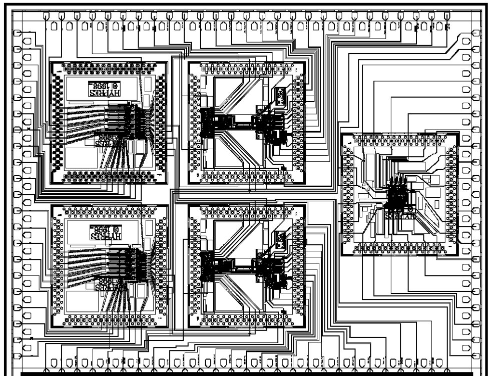
Transient Digitizer: Two 6-bit 20 GSa/s Flash ADCs with 32-word memory



Two-channel Dual-function Digitizer (TDC & ADC)



Two-channel Digital Channelizer (>12,000 JJs)



Multi-chip Module (20 Gbps interchip data rate)

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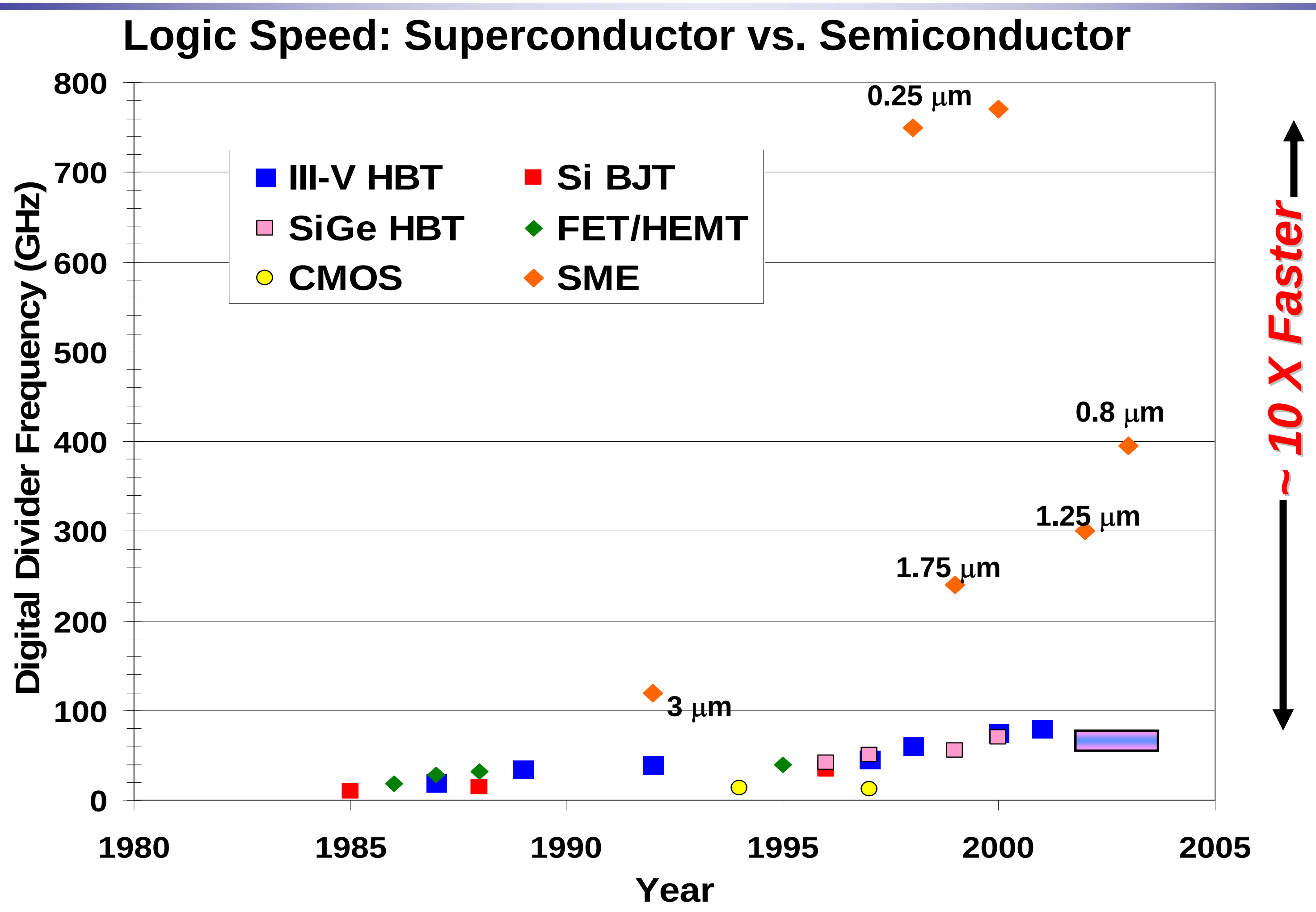
Benchmark Performance Metric for Digital Logic



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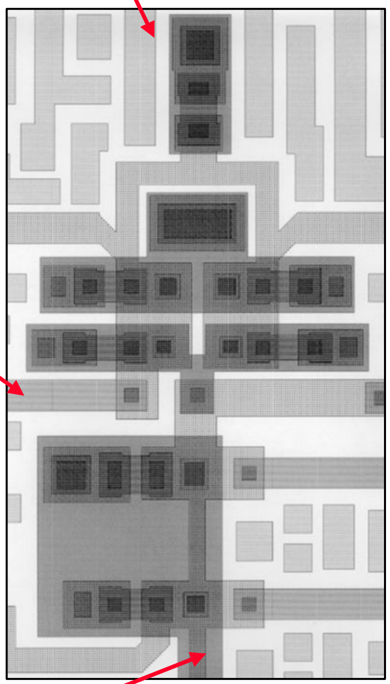
120 GHz Operation of a Toggle Flip-Flop (3-µm)

Output

Current bias



Input

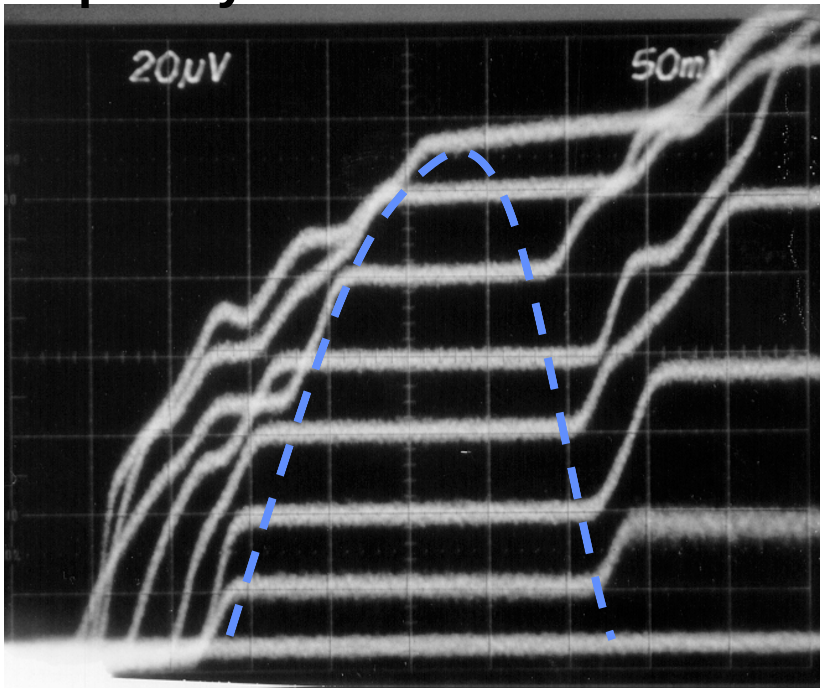
Input Frequency GHz

120

80

40

0

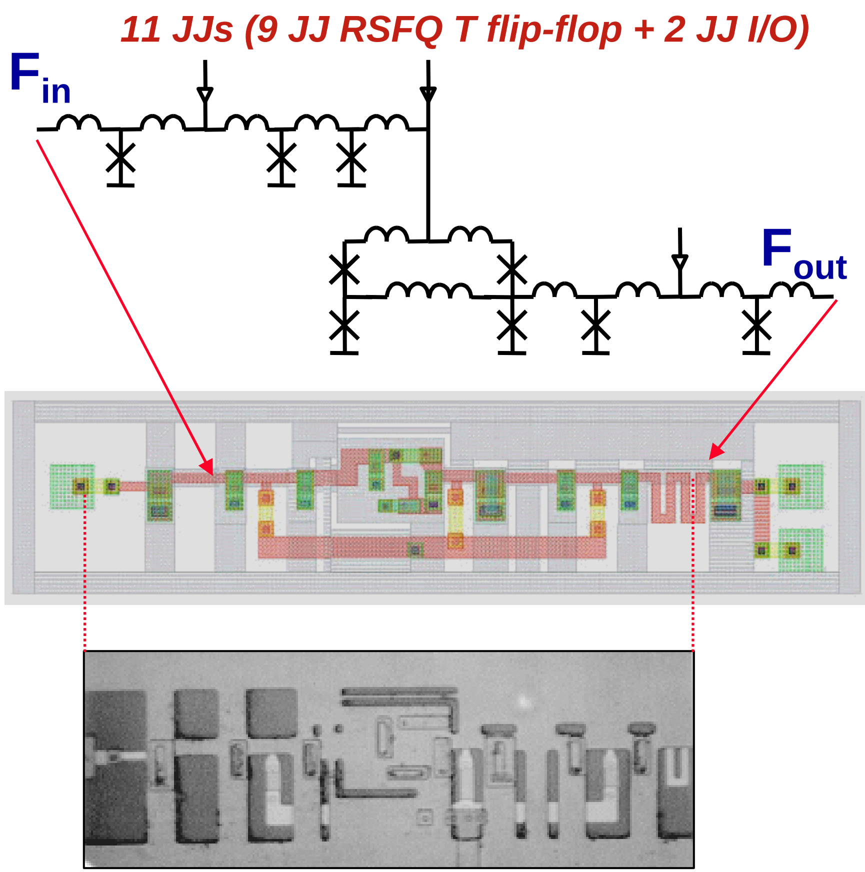


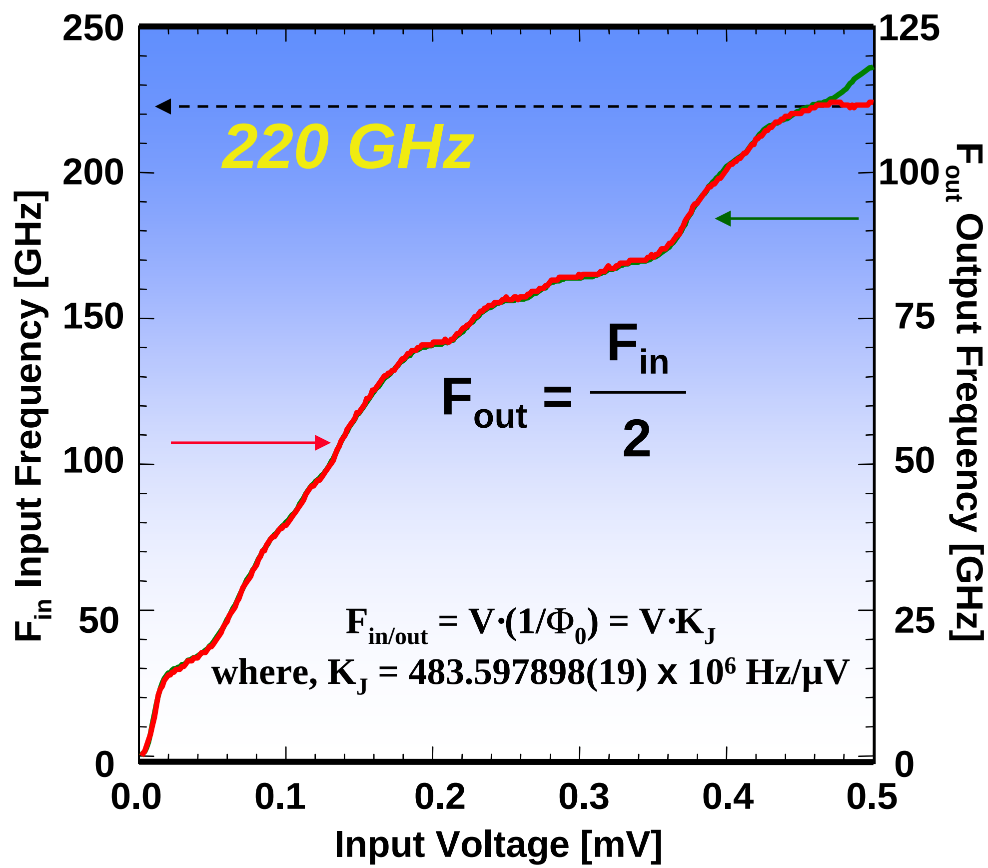
Current Bias

Operational Region at Different Input Frequencies
(set of output voltages vs. current supply)

HYPRES

220 GHz Operation of a Toggle Flip-flop (1.75-µm)

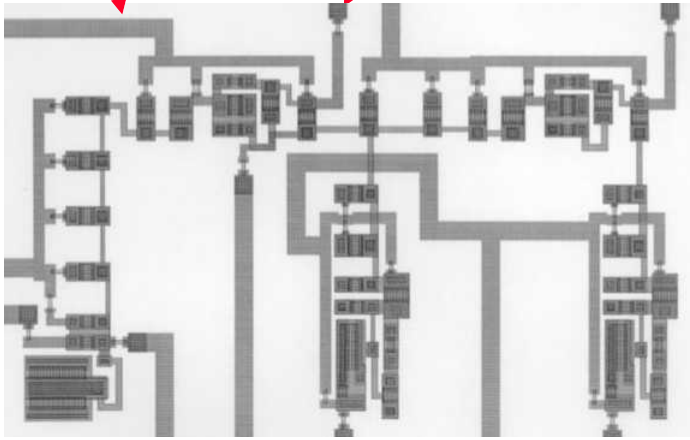


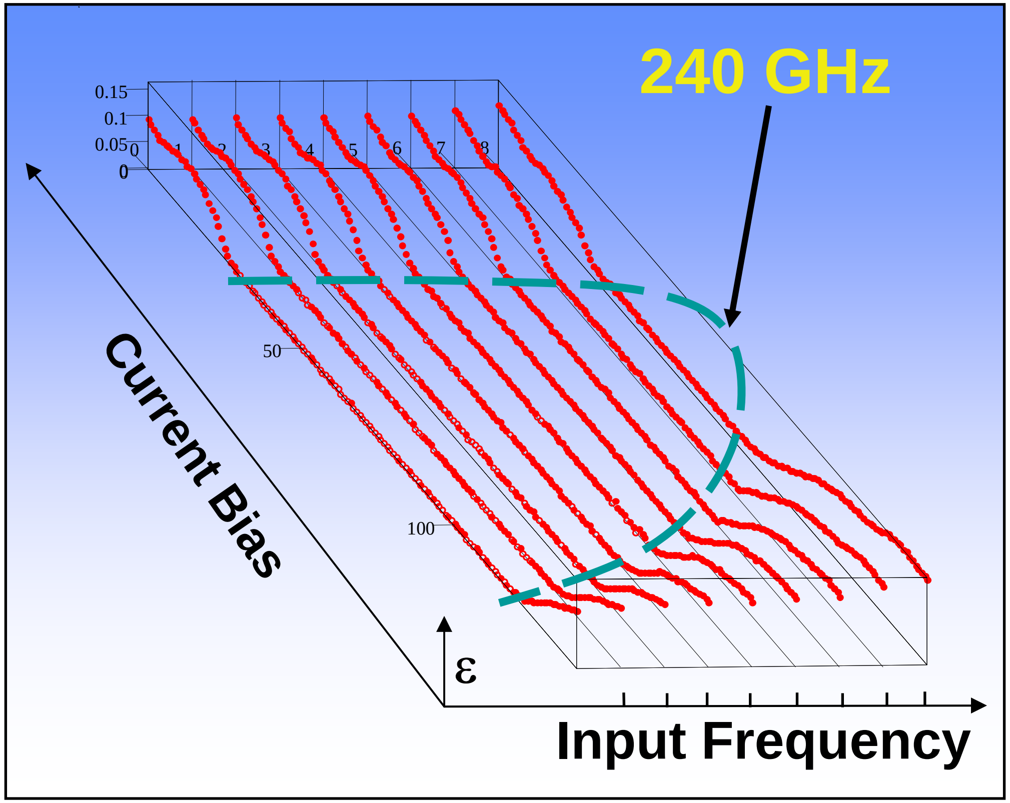


HYPRES' 1.75-µm, 5 kA/cm², CMP Nb Josephson fabrication process

HYPRES

240 GHz Operation of a Toggle Flip-flop (1.5-µm)



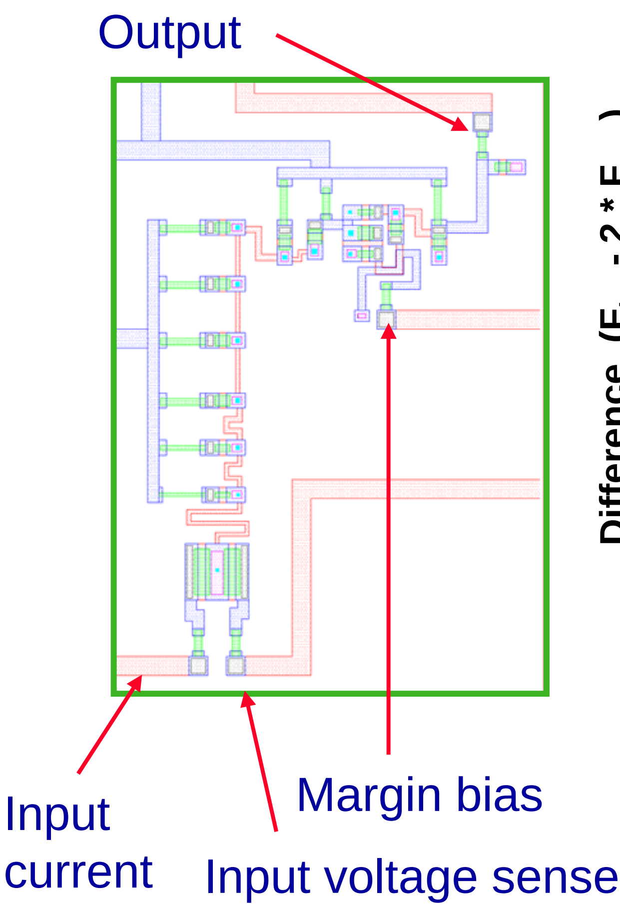


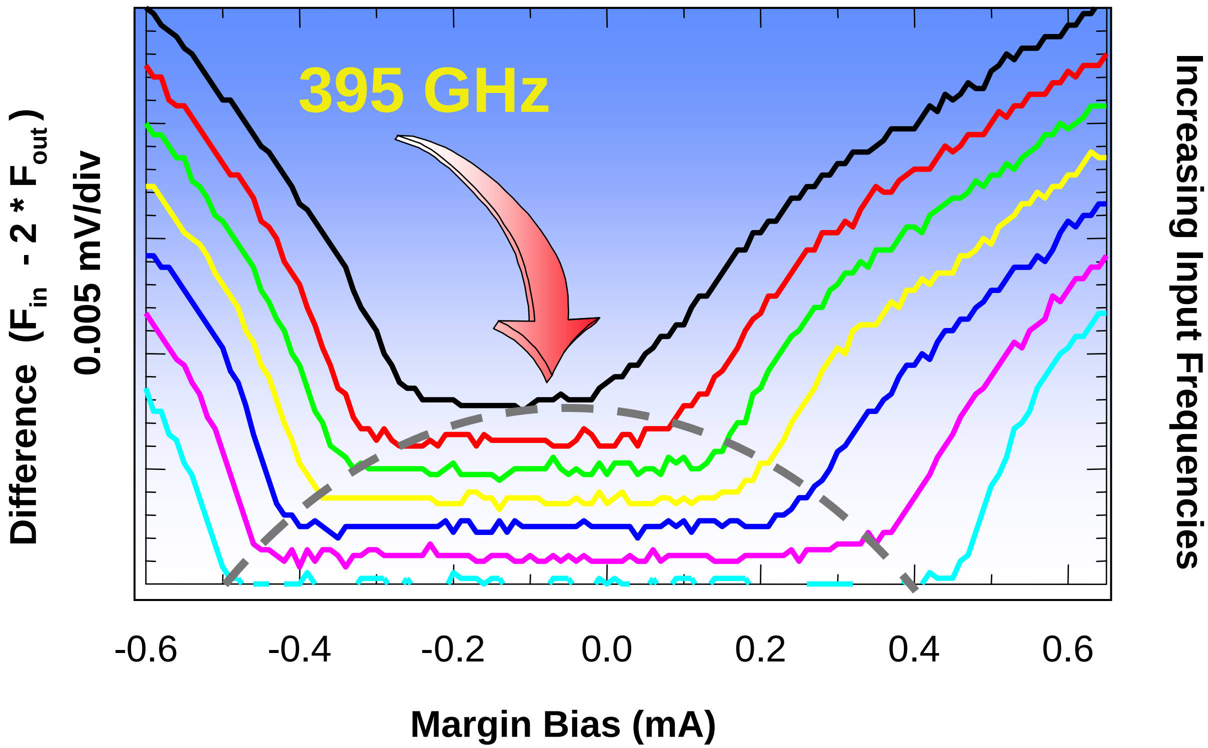
Operational Region at Different Input Frequencies (set of voltage differences vs. current)

SUNY' 1.5-µm, 6 kA/cm², CMP Nb Josephson fabrication process

HYPRES

395 GHz Operation of a Toggle Flip-flop (0.8-µm)



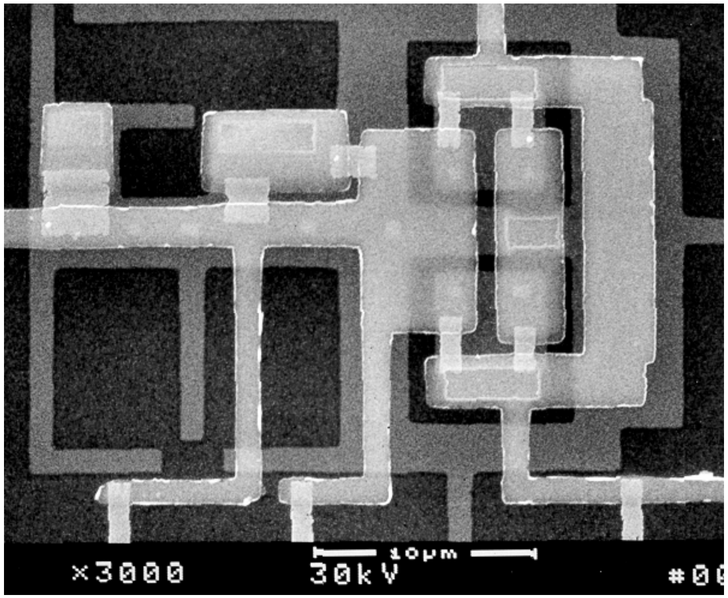


Operational Region at Different Input Frequencies (set of voltage differences vs. current)

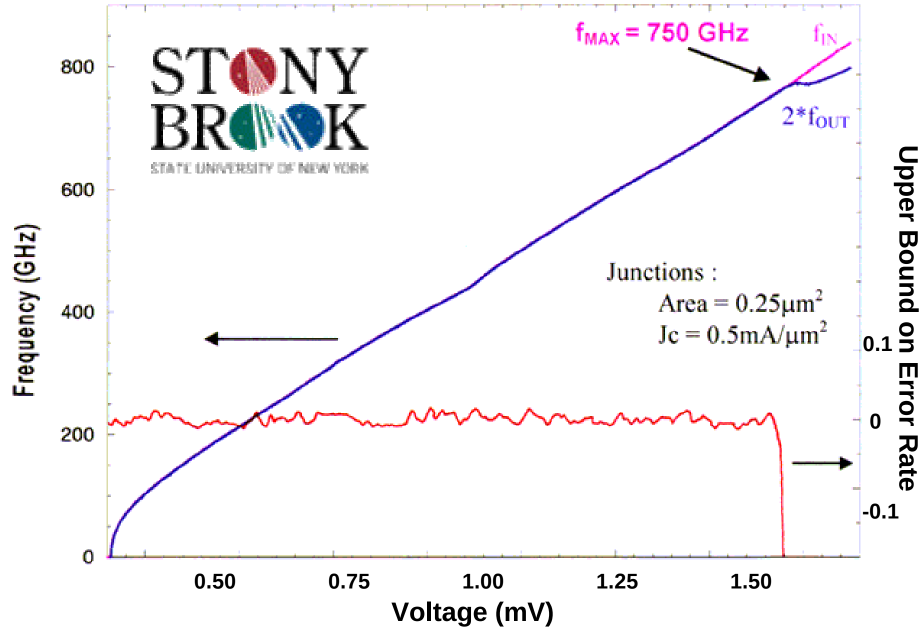
SUNY' 0.8-µm, 20 kA/cm^2, CMP Nb Josephson fabrication process

HYPRES

750 Gb/s RSFQ Digital Frequency Divider



0.25-μm Nb Fabrication Process



DFD operation for $f_{OUT} = \frac{1}{2} f_{IN}$

NIST CERTIFIED

Fundamental Physical Constant

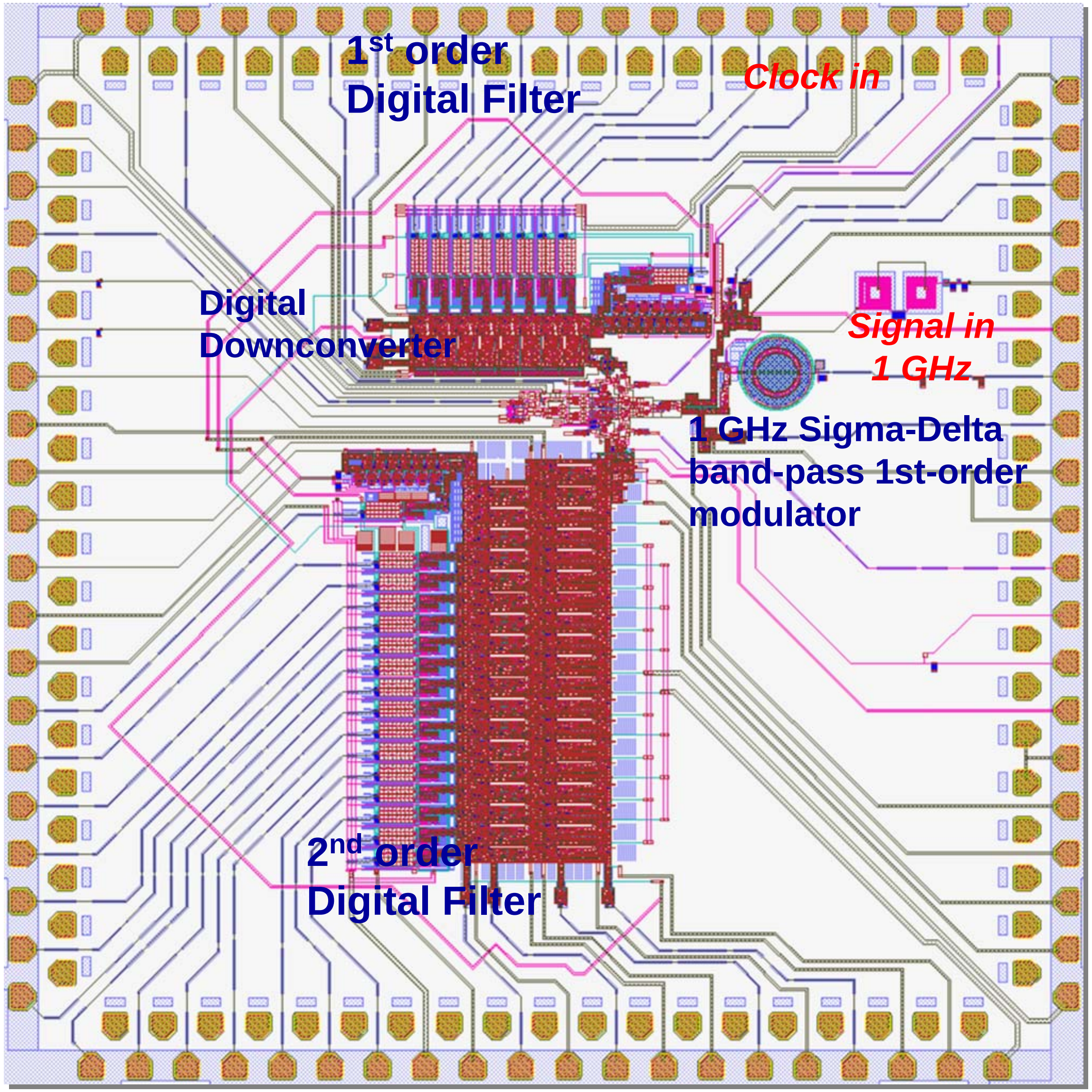
$V = \Phi_0 \cdot f_J$ $\downarrow$ [bits / second] - or - $f_J = V \cdot (1/\Phi_0) = V \cdot K_J$

where, $K_J = 483.597898(19) \times 10^6$ Hz/μV [accuracy 0.39 ppb]

SUNY' 0.25-μm, 140 kA/cm², CMP Nb Josephson fabrication process

HYPRES

A 1 GHz Band-Pass ADC Test Chip

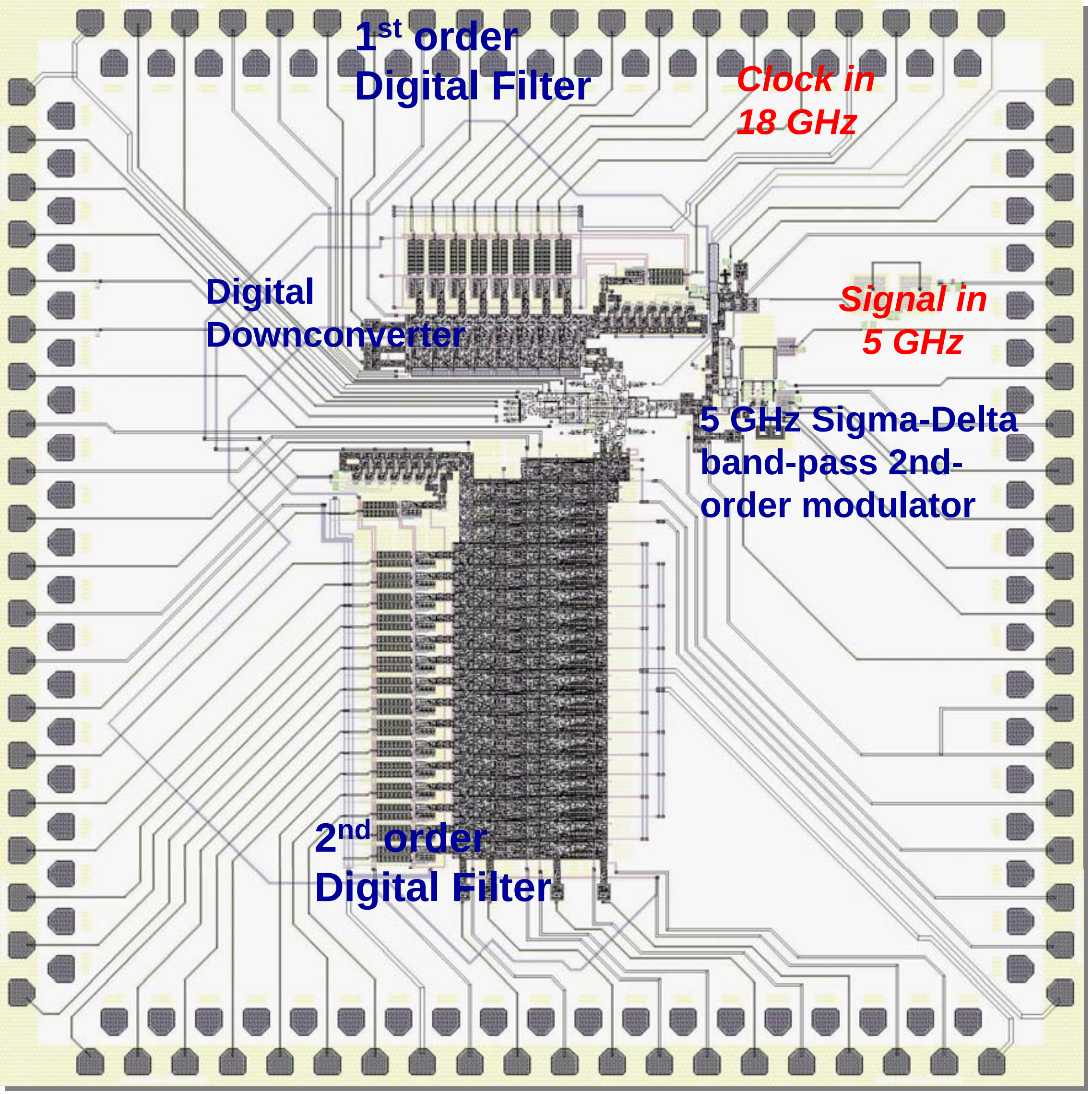


- 3 micron process, 20 GHz clock
- Two digital filters:
  - 1st order 8-bit filter
  - 2nd order 15-bit filter

High-Speed Functionality has been successfully proven: 1 GHz signal has been directly digitized and digitally downconverted to baseband

HYPRES

A 5 GHz Band-Pass ADC Test Chip

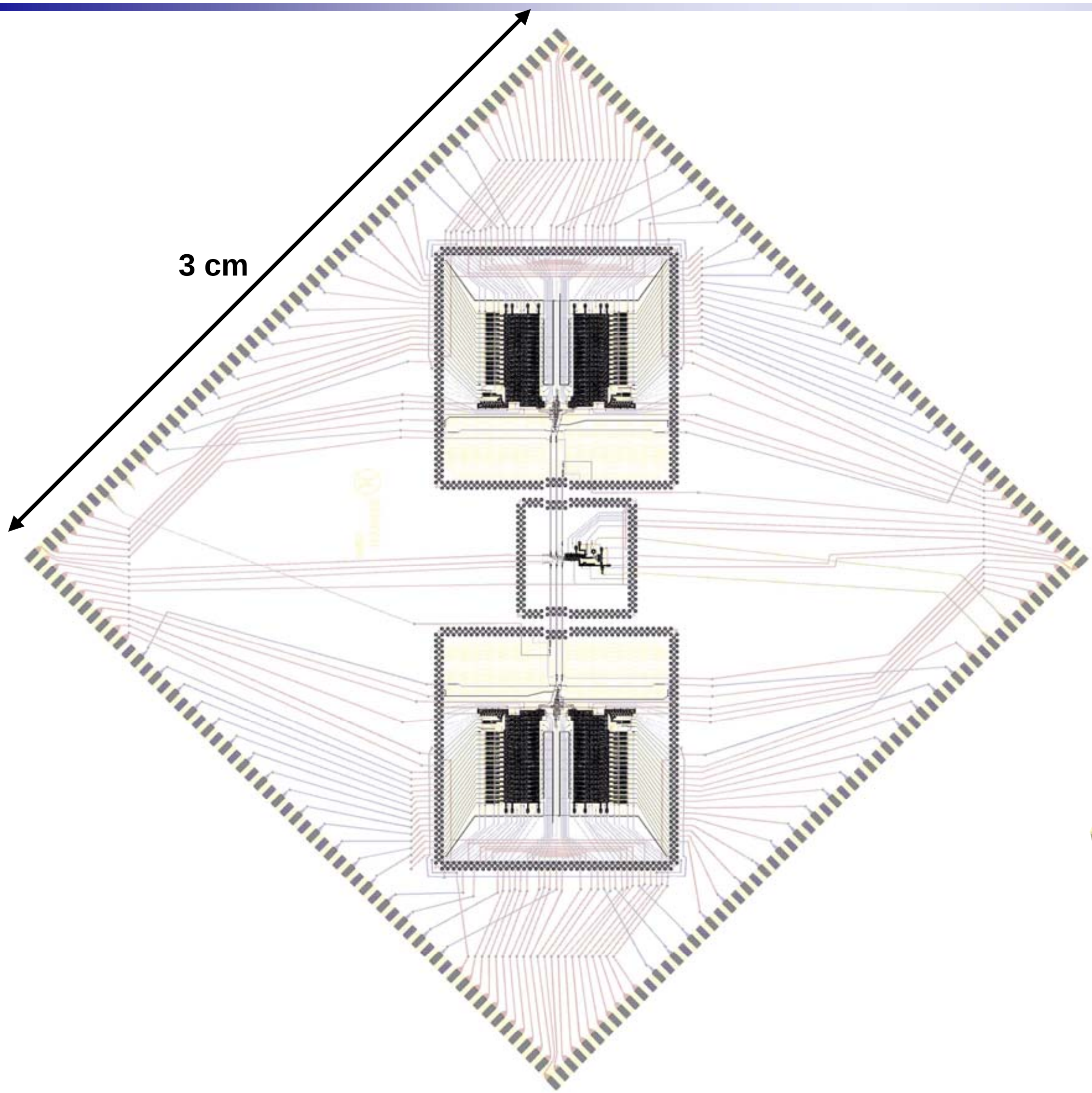


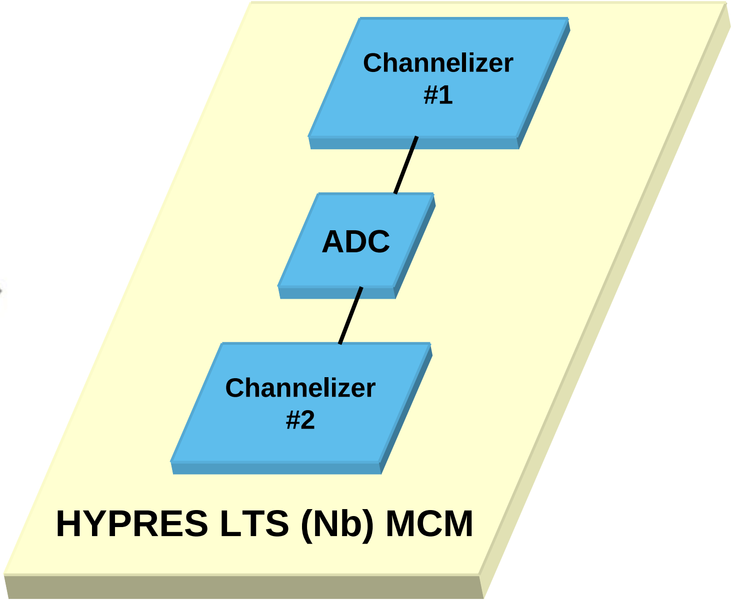
- 3 micron process, 20 GHz clock
- Two digital filters:
  - 1st order 8-bit filter
  - 2nd order 15-bit filter

High-Speed Functionality has been successfully proven: 5 GHz signal has been directly digitized and digitally downconverted to baseband

HYPRES

Two-Channel Digital-RF Receiver MCM





HYPRES

Cryocoolers
&
Cryopackaging

HYPRES

Cryocooler Choices/Advantages

- Key enablers of high performance, demonstrated in:
  - Wireless cellular communications (HTS filters)
  - Mine detection
  - Highest sensitivity radar receivers
  - IR imaging systems
- Proven to meet any and all requirements as designed:
  - Reliability (demonstrated MTBF of 90+ years)
  - Ruggedness (proven in space environment)
  - Combat environment (proven in IR imaging systems)
  - Efficiency (MEMS package)
- Multiple vendors (ready to perform) and approaches leading to competitive choices and selection:
  - Commercial vendors (Leybold, Air Liquide, Sumitomo)
  - Military contractors (Ball Aerospace, Lockheed Martin)
  - Small Business (TAI, Sunpower, Creare)

Performance/Reliability far exceeding conventional electronics

HYPRES

Cryocoolers in Use

- Cryocooled superconducting filters fielded today in **military systems**
  - Conforms to all military specifications
- Cryocooled superconducting filters fielded today in **commercial cellular base stations**
  - 99.999% Uptime, MTBF of 90+ years
- Cryocoolers **deployed in space**
  - Passed space qualification
- Cryocoolers used in vacuum systems in **semiconductor foundry**
  - Conforms to highest reliability requirements

HYPRES

Demonstrated Reliability

20,000,000

~~11,200,000~~

~~6,300,000~~

~~3,500,000~~

~~1,600,000~~ hours of operation

Demonstrated MTBFs of 90+ years!!

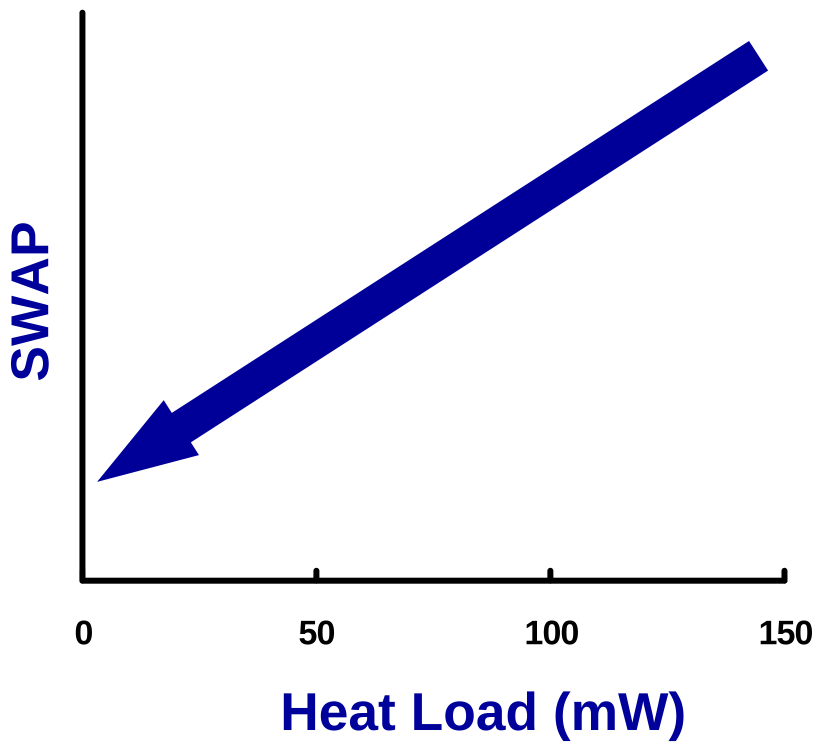
Estimated uptime of 99.999%

HYPRES

Multiple Approaches to Heat Load Reduction

- **HTS leads** provide excellent electrical conductance and reduced thermal conductance
- **Output multiplexing** reduces number of output leads
- **Bias current recycling** reduces number of DC Bias lines
- Radiation load can be reduced by use of **intermediate temperature shields**

Size, Weight, And Power (SWAP) vs. Heat Load



HYPRES

Progression Path

Minimize size, weight and power of the cryocooler

Past 2 kW

19" x 5 ft

Present ~ 1.3 kW

~~**Near Term < 1.5 kW**~~

~~**19" x 2 ft**~~

19" x 16"

150 – 300 W

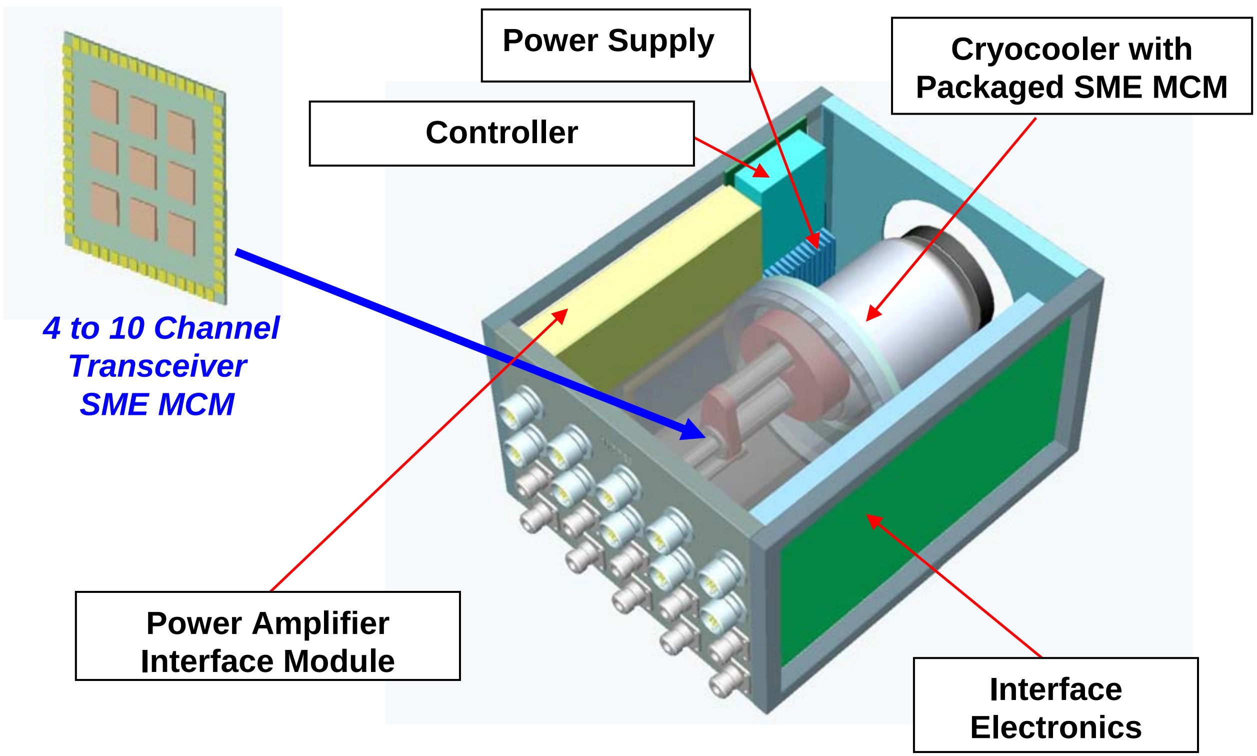
10-channel Military Tx/Rx

Multi-channel Commercial Tx/Rx

250 – 500 cu.in.

HYPRES

Digital-RF Transceiver

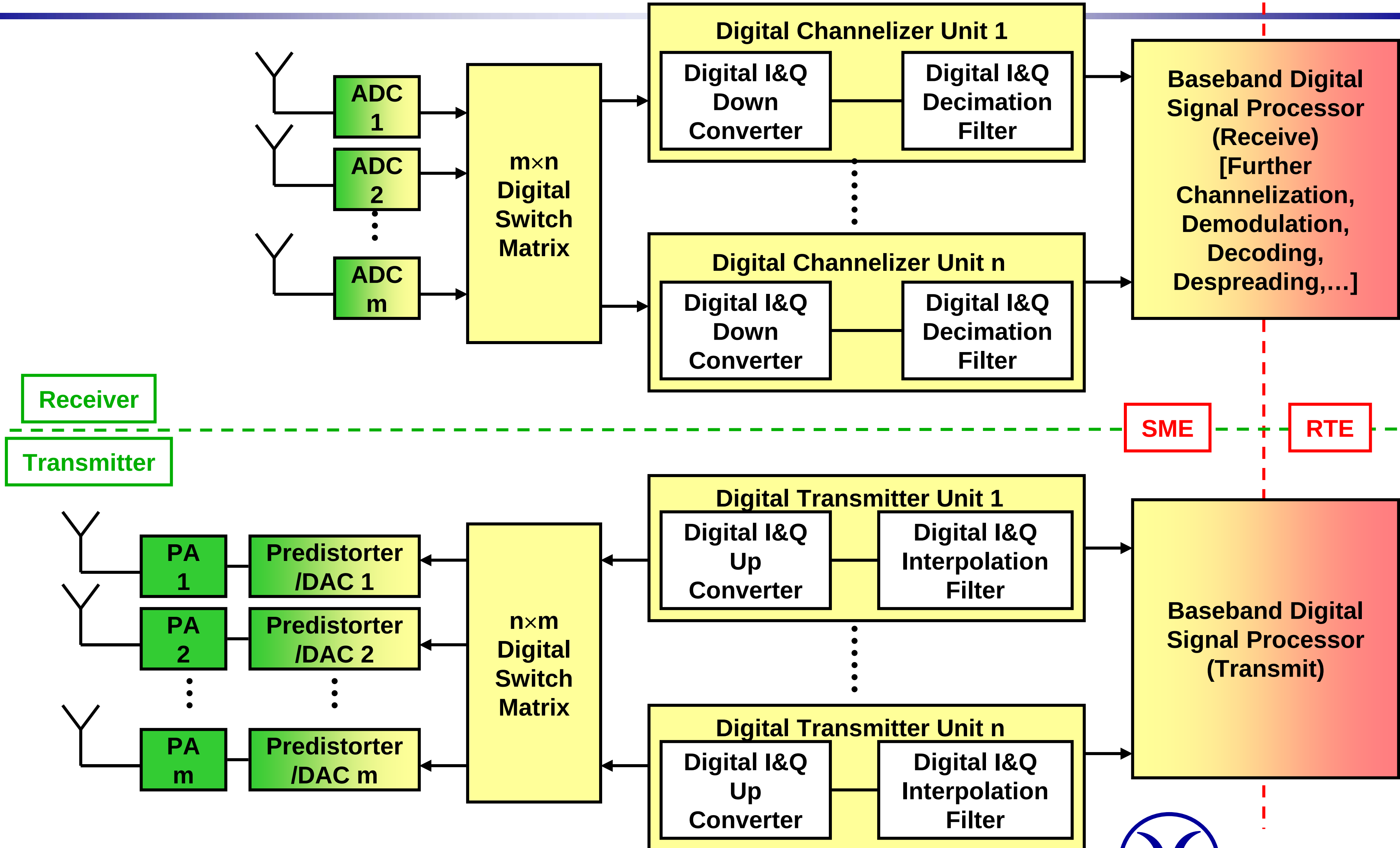


6” x 8” x 10” = 480 in^3
[for 10 channels]

HYPRES

Generic Digital-RF Transceiver

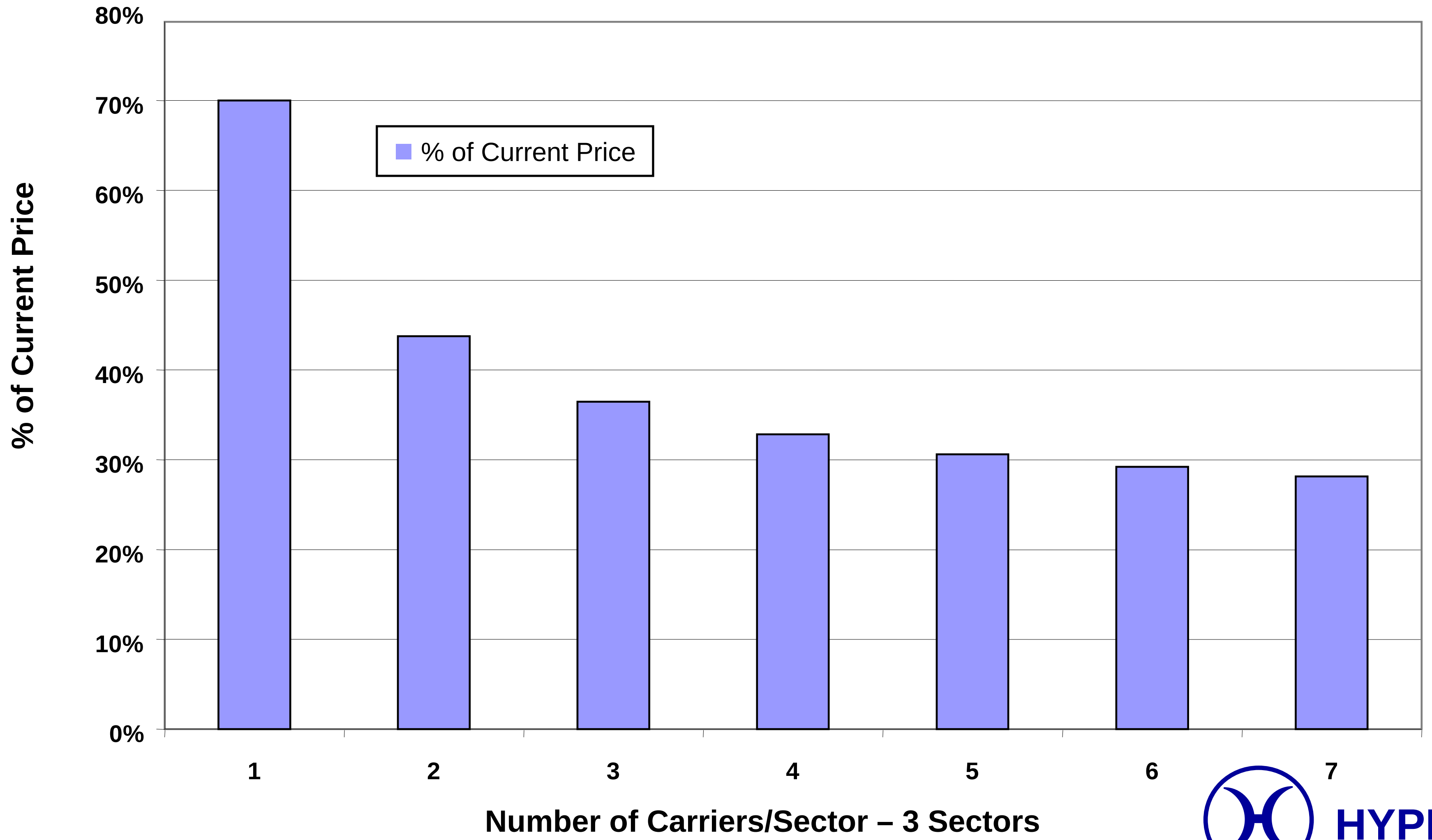
[JTRS]



HYPRES

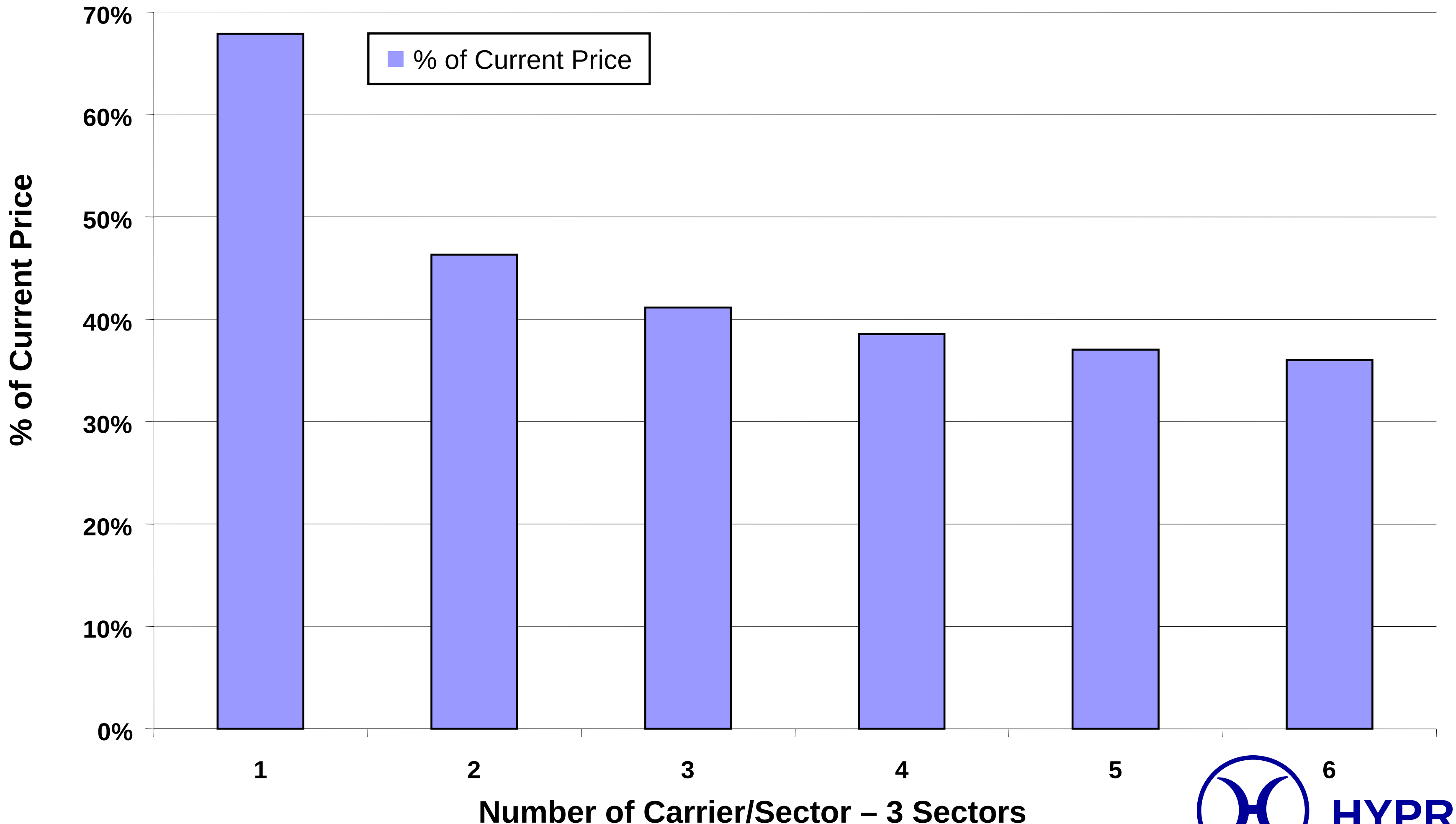
Note: For a (JTRS) 10-channel 2-2000 MHz transceiver, n = 10, m = 3 to 5

% of Current Price -- CDMA



HYPRES

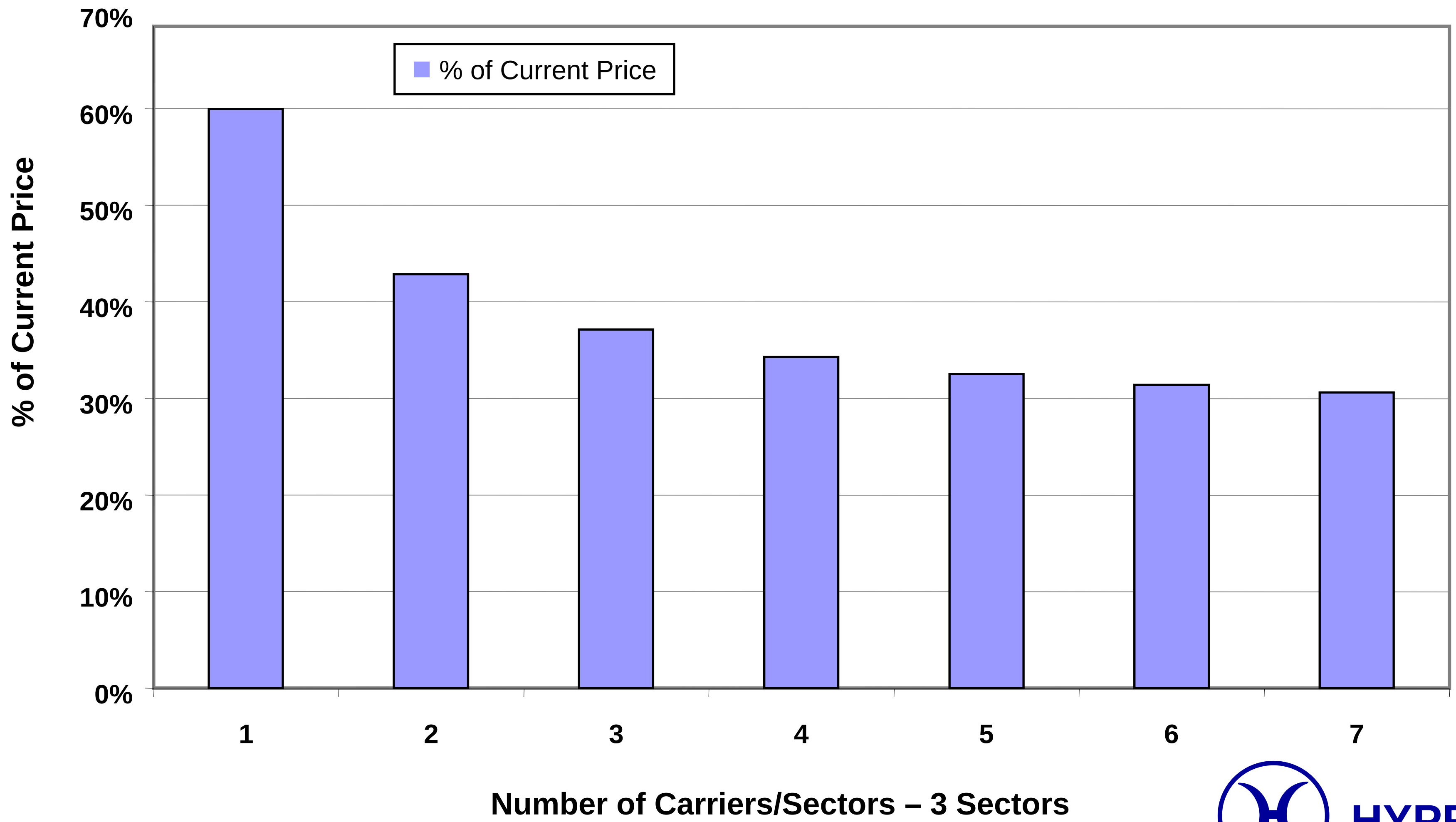
% of Current Price -- GSM



HYPRES

% of Current Price – UMTS (WCDMA)

[and TD-SCDMA]



HYPRES

HYPRES Product Benefits for Wireless Networks

Summary

- **Massively Reduced Network Capital Expenditures**
  - Much Fewer Base Stations
  - Lower Capitalization per Base Station
  - Postponement (“one size fits all”– “air interface immune”)
- **Substantially Reduced Operating Expense**
- **Enhanced Revenues and Margins**
- **Significantly Enhanced Performance**
- **Unparalleled Reliability & Flexibility**
- **A “Natural” for Distributed Radio (over fiber, etc.)**
- **Boost Spectral Efficiency (HSDPA, etc.)**
- **Future-Proof Products -- beyond 3G (>30Mb/s inherent)**
- **Extended Mobile Battery Life/Throughput**

HYPRES Digital-RF enables the next generation Base Station

HYPRES

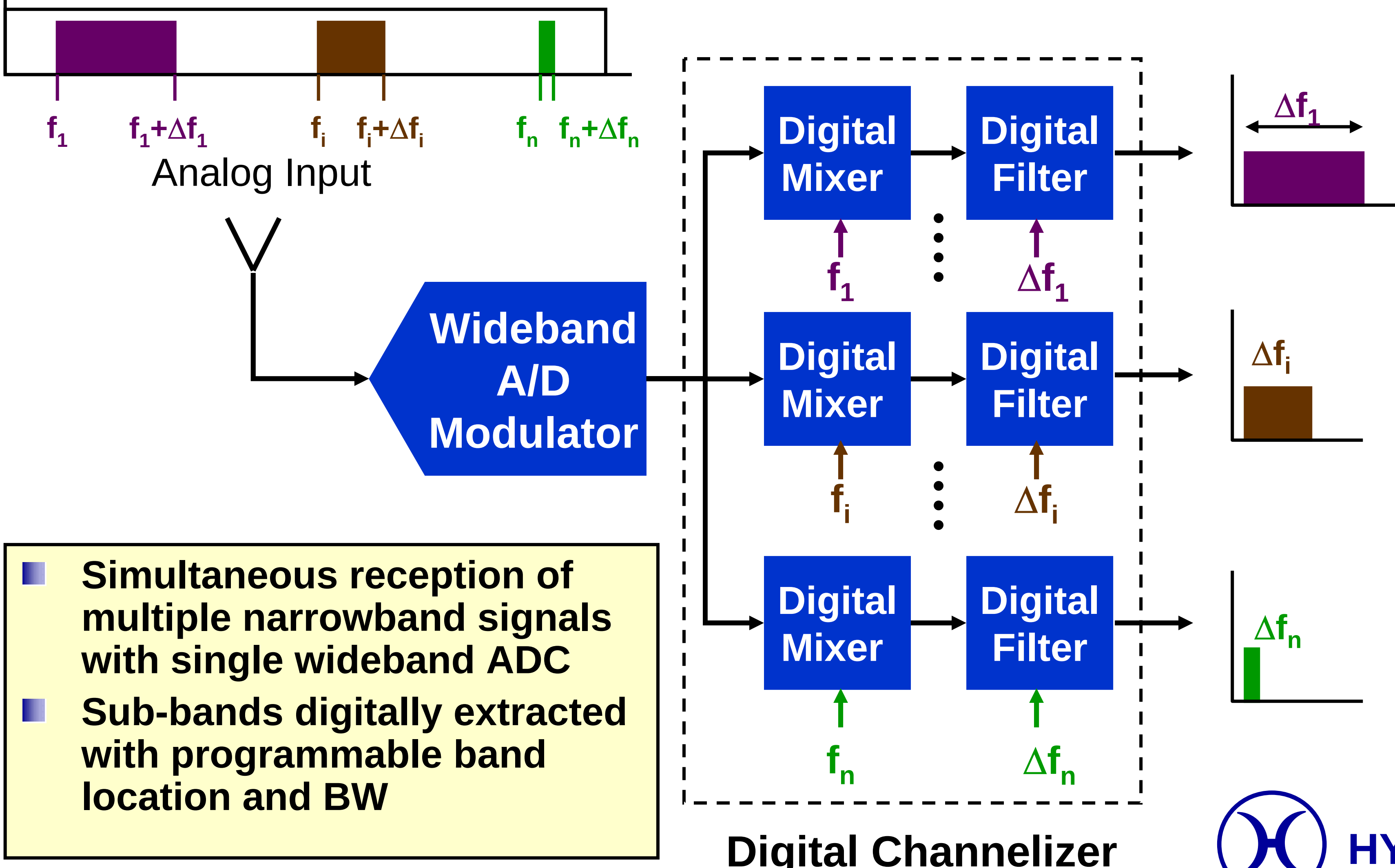
HYPRES SME Technology

Brings the Power of Digital Processing to the RF Domain and changes the Paradigm of Wireless Communications

Additional Information

Wideband Digital-RF Channelizing Receiver

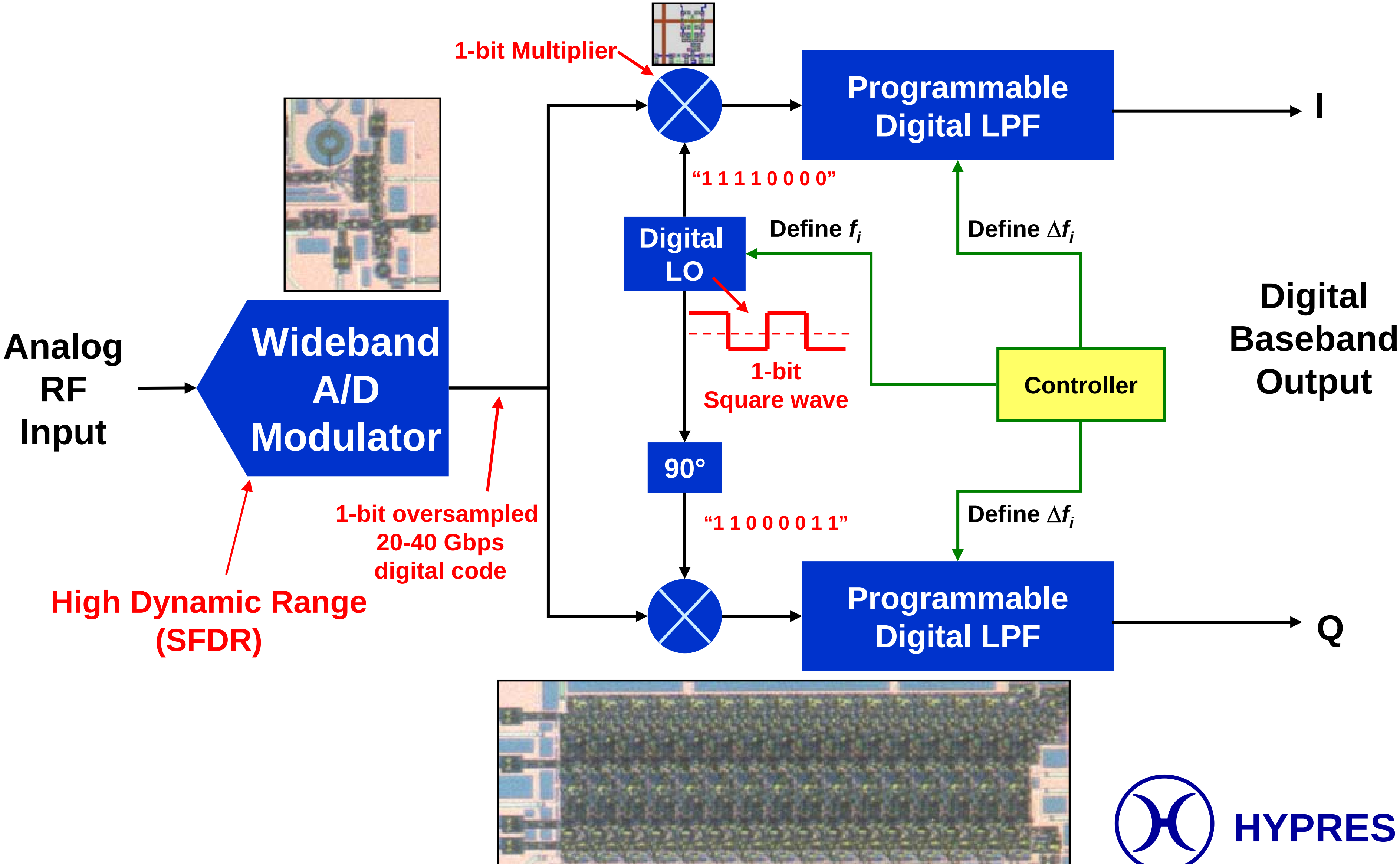
Programmable Band-location and Bandwidth Selection



- **Simultaneous reception of multiple narrowband signals with single wideband ADC**
- **Sub-bands digitally extracted with programmable band location and BW**

HYPRES

Digital Processing at RF Frequencies [RF DSP]

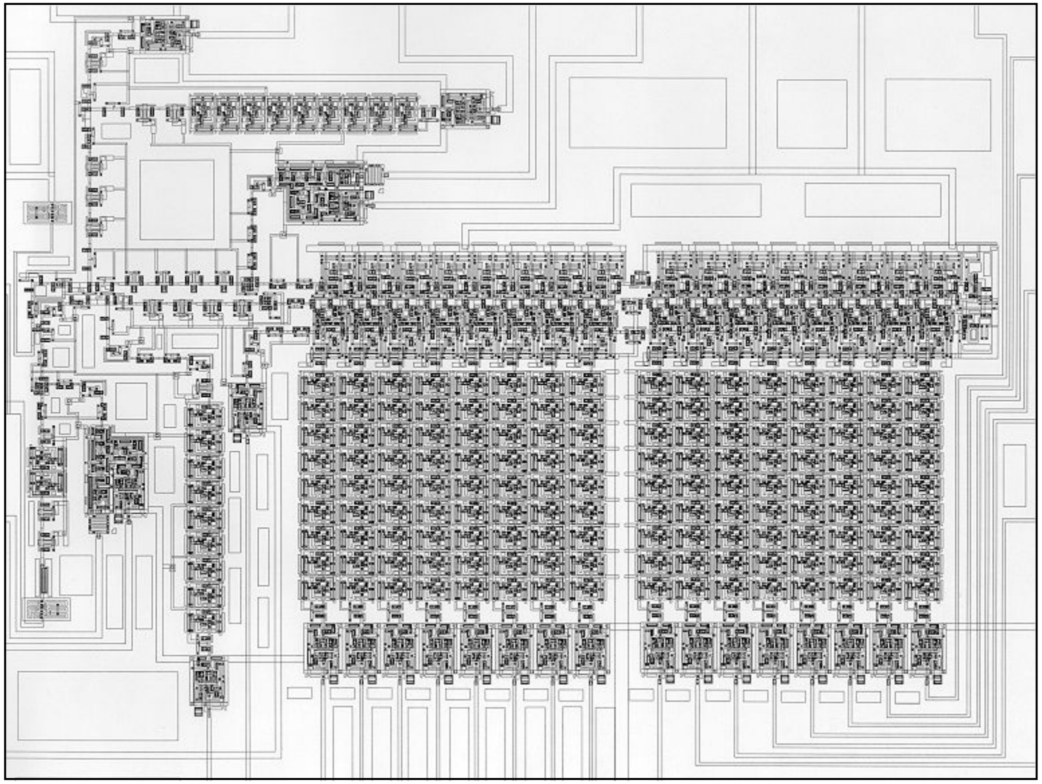


HYPRES

Demonstrated Digital Autocorrelator

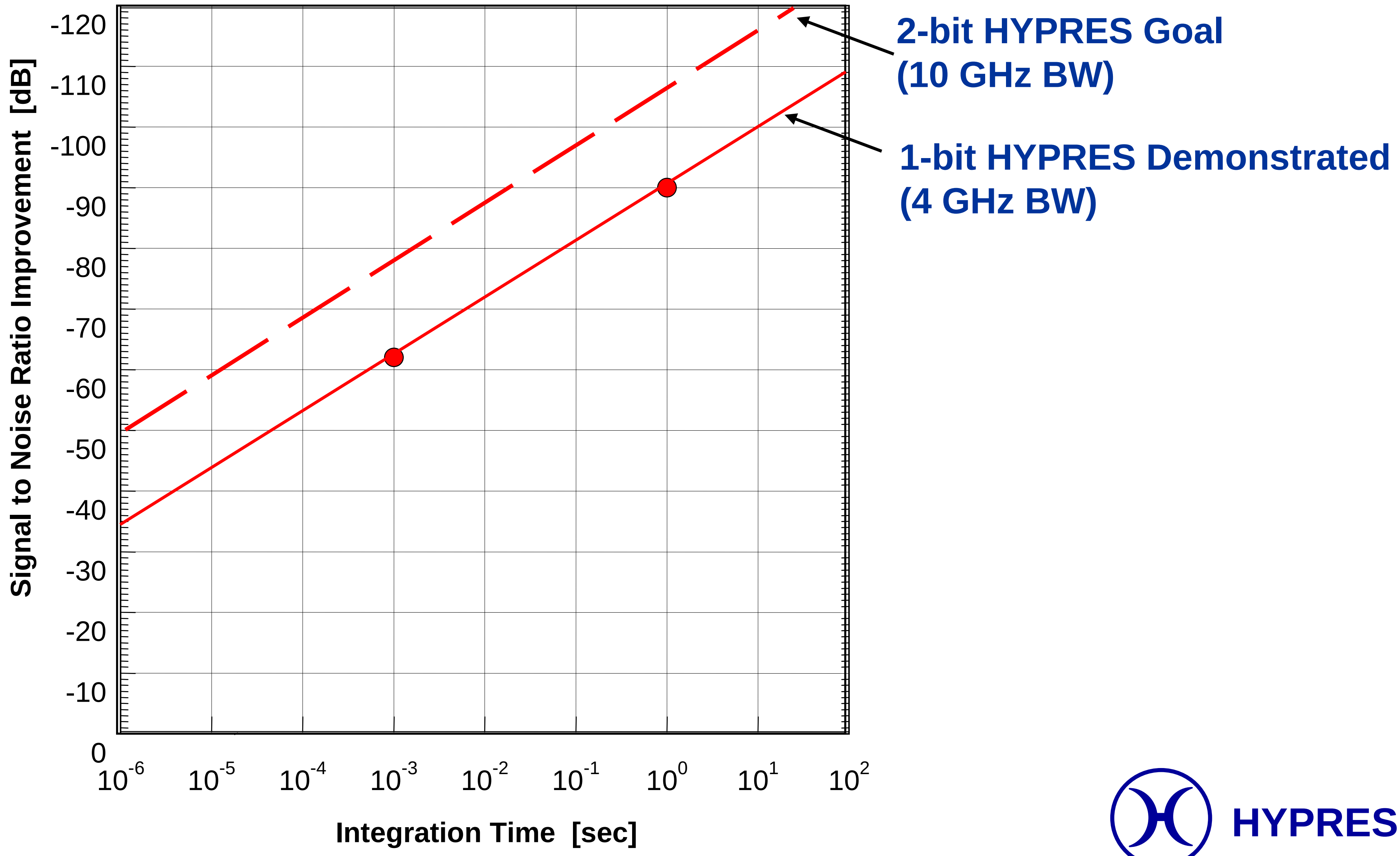
- 4 GHz bandwidth /16 GHz clock
- 16 correlator channels
- 9-bit output values
- 1600 devices
- 5 mm x 5 mm chip size
- DSP blocks include
  - Multipliers
  - Accumulators
  - Adders

[Result of a Phase I STTR]



HYPRES

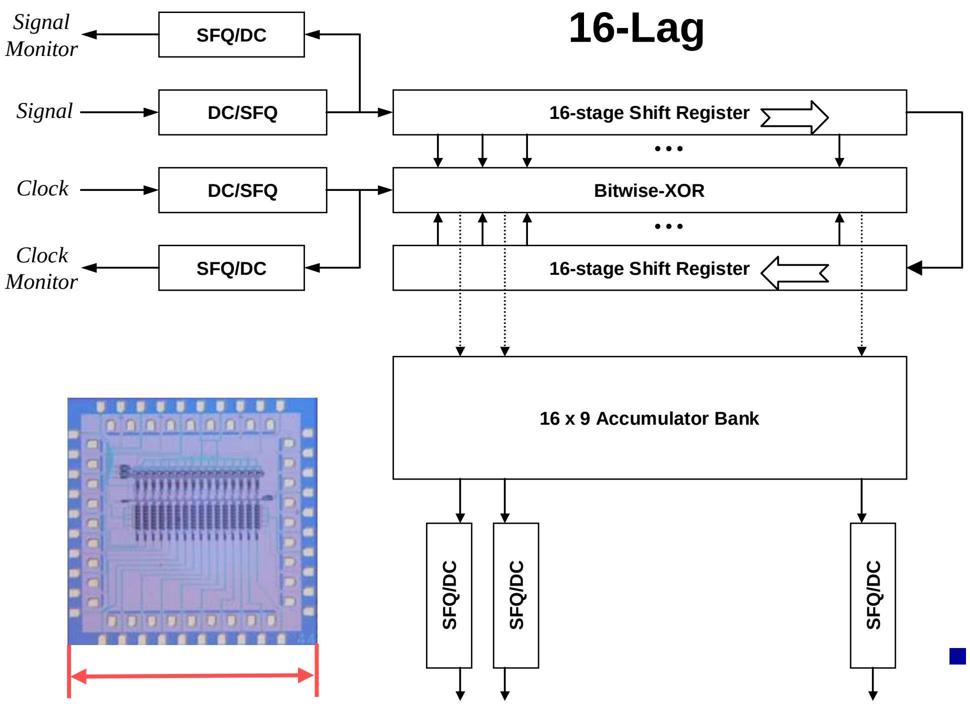
Autocorrelator Performance



HYPRES

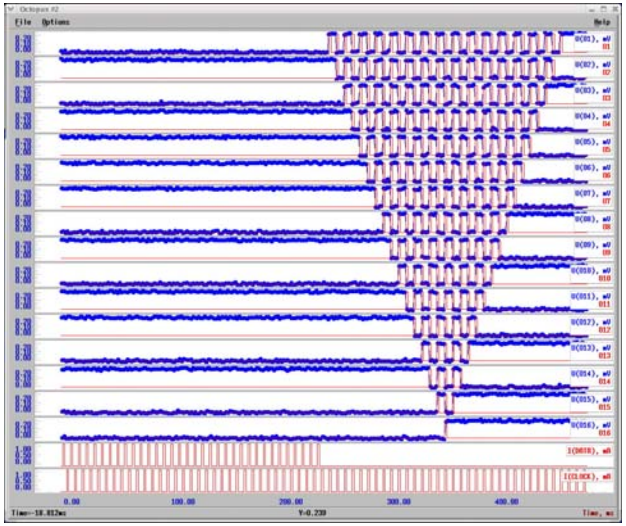
Digital Autocorrelator

16-Lag



5 mm

"it works"

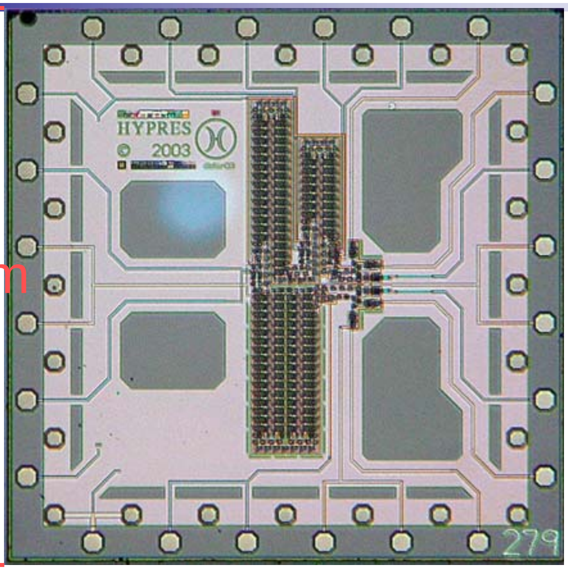


- Test sequence when a train of 2X16+2=34 '1's (signal "DATA") is loaded into the circular shift register.
- The correct operation of all 16 XOR gates for all possible combinations of inputs ("00", "10", "01", "11") and correct operation of circular shift register under full load.

HYPRES

Programmable 112-bit Shift Register

5 mm



~ 1500 JJs

"it works"

Data output after 16 cycle delay with S0=S3=S5=1 and S1=S2=S4=0 →

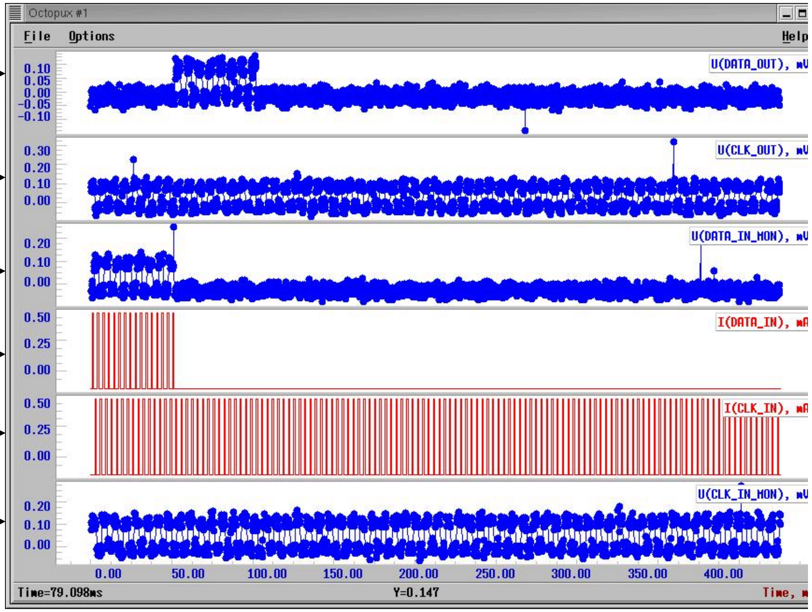
Clock output →

Data input monitor →

Data input →

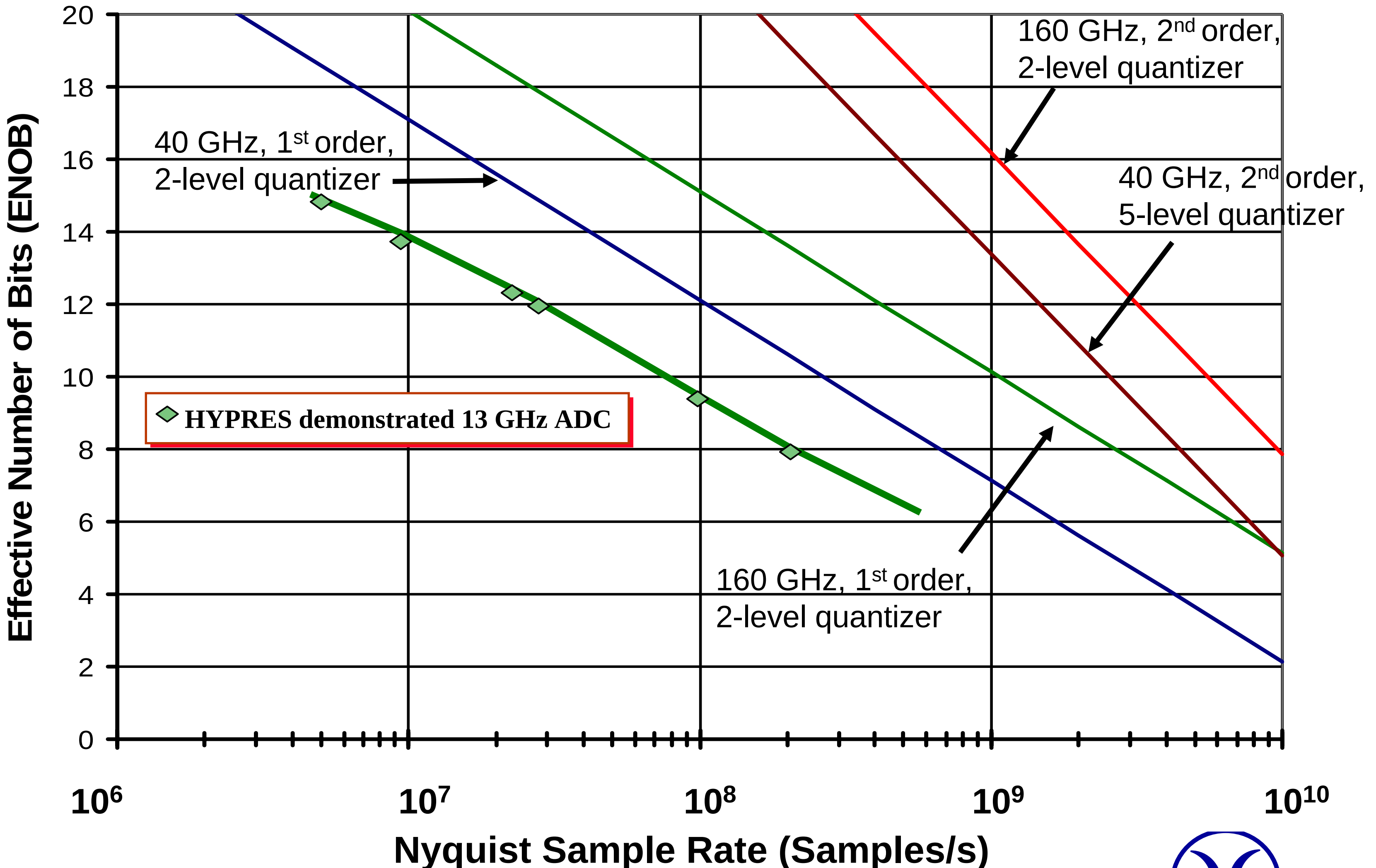
Clock input →

Clock input monitor →



HYPRES

ADC Performance Enhancement

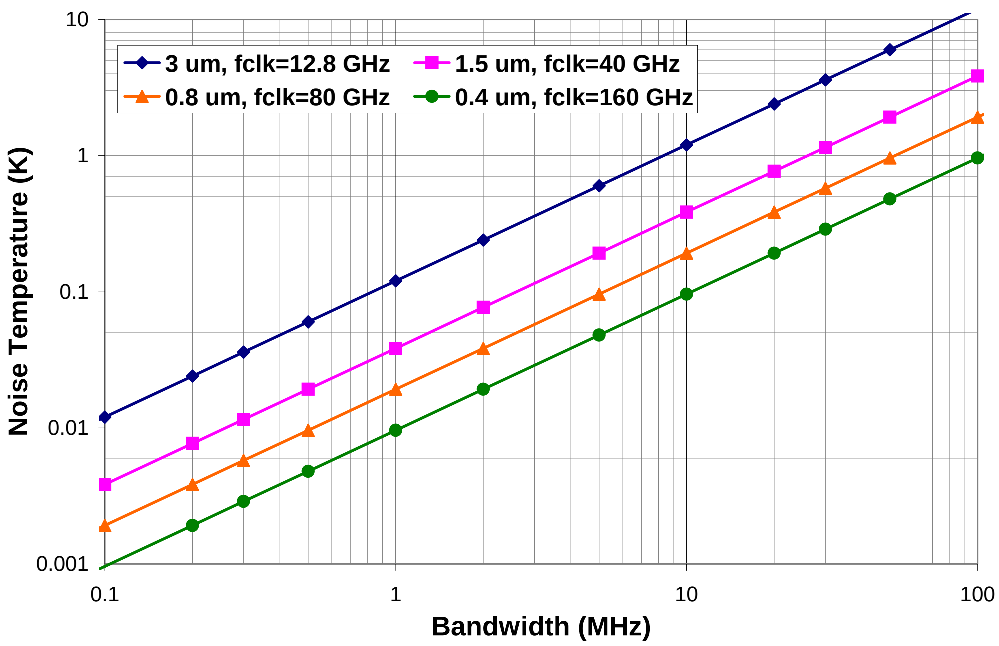


HYPRES

Ultra-low ADC Noise

- At 5 K, thermal noise is 60x less than at room temperature
- ADC only produces a "quantization error" (I_N)
- With dither, I_N has a noise-like spectrum
- Noise Temperature (T_N)

$$T_N = \frac{(I_N)^2 R}{k_B f_s} = \frac{\pi}{12 k_B L_2}\left(\frac{\Phi_0}{km}\right)^2 \frac{\Delta f}{f_{clk}} \propto \frac{\Delta f}{f_{clk}}$$



- L_2 = Front-end inductance
- m = # of synchronizer channels
- f_{clk} = Clock frequency
- Δf = signal bandwidth

ADC does not degrade the system noise temperature

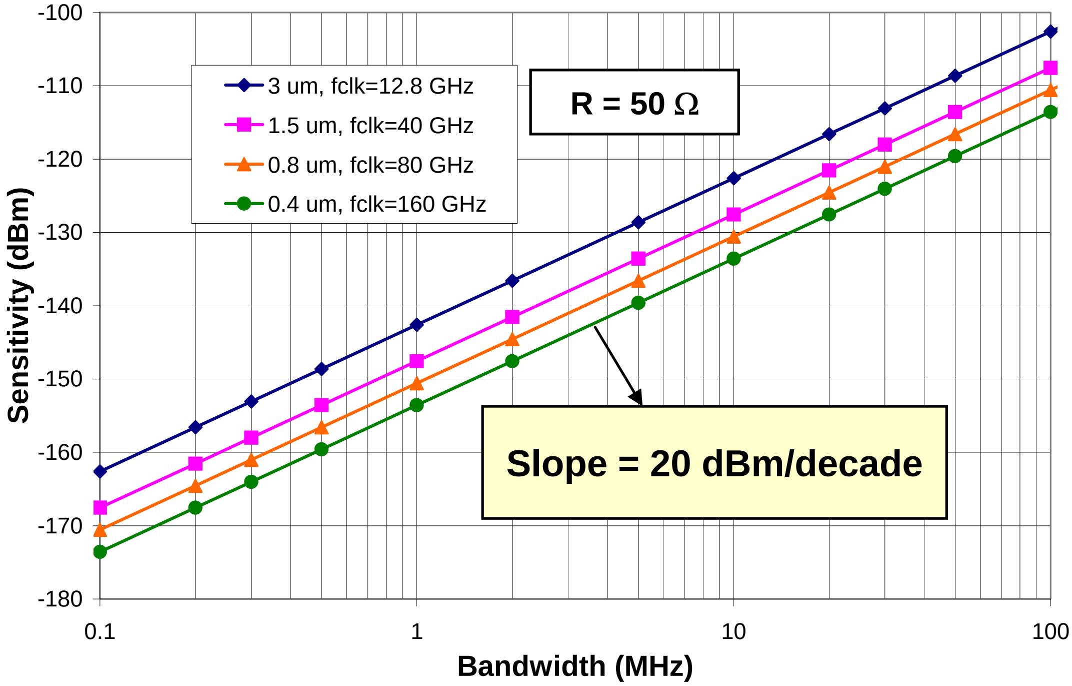
HYPRES

Ultra-high ADC Sensitivity

- Sensitivity (ΔI) is the least significant bit (LSB)

$$\Delta I = \frac{\Phi_0}{2Mm\sqrt{N}} \propto \frac{\Delta f}{\sqrt{f_{clk}}}$$

$$(\Delta I)^2 R \propto \frac{(\Delta f)^2}{f_{clk}}$$

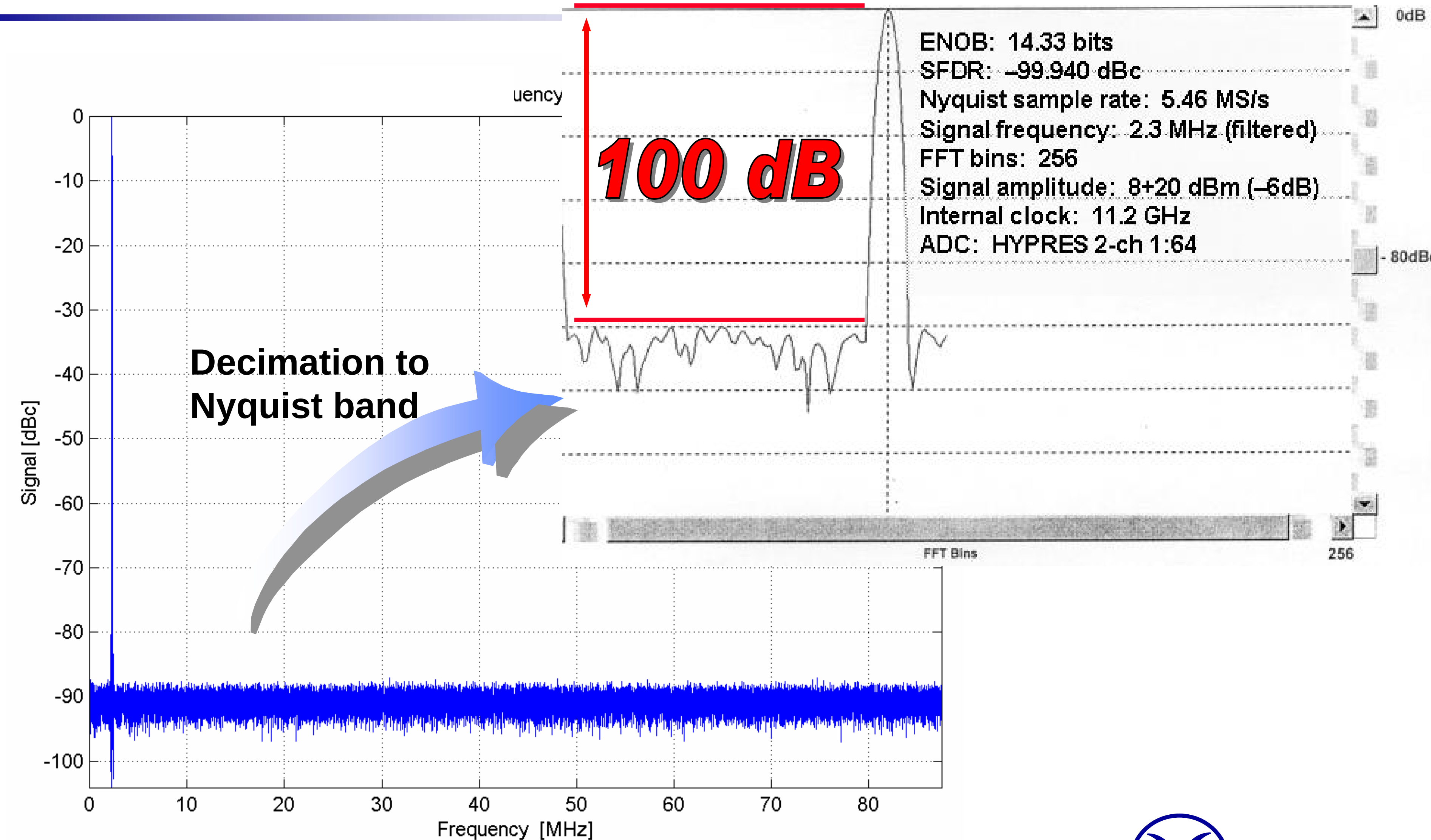


- M = Mutual inductance
- m = Number of synchronizer channels
- f_{clk} = Clock frequency
- Δf = signal bandwidth
- N = Oversampling ratio = $f_{clk}/(2f_s)$

SQUID, used as ADC front-ends, is <u>the</u> most sensitive energy detector

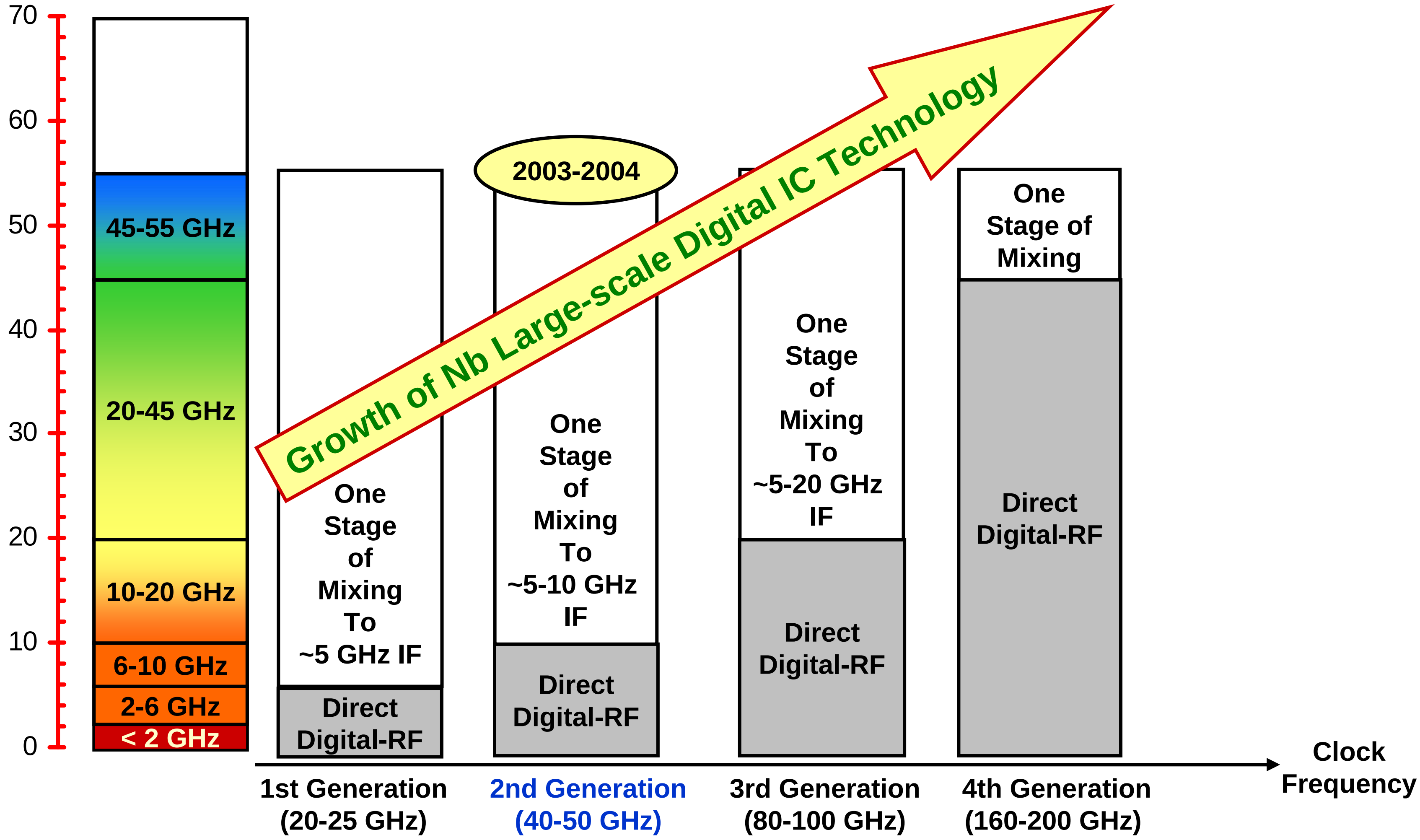
<u>~ 60dB better than conventional</u>

Deep FFT Measurements Show >100 dB SFDR



HYPRES

Technology Growth



Digital-RF: Digitization and Digital Processing at multi-GHz RF

HYPRES

RSFQ

HYPRES Technology

HYPRES SME technology is
so accurate that it defines the Volt,
so sensitive that it measures brain currents,
so fast that it directly converts RF signals.

Based on a naturally occurring periodic quantum effect — Rapid Single Flux Quantum (RSFQ)

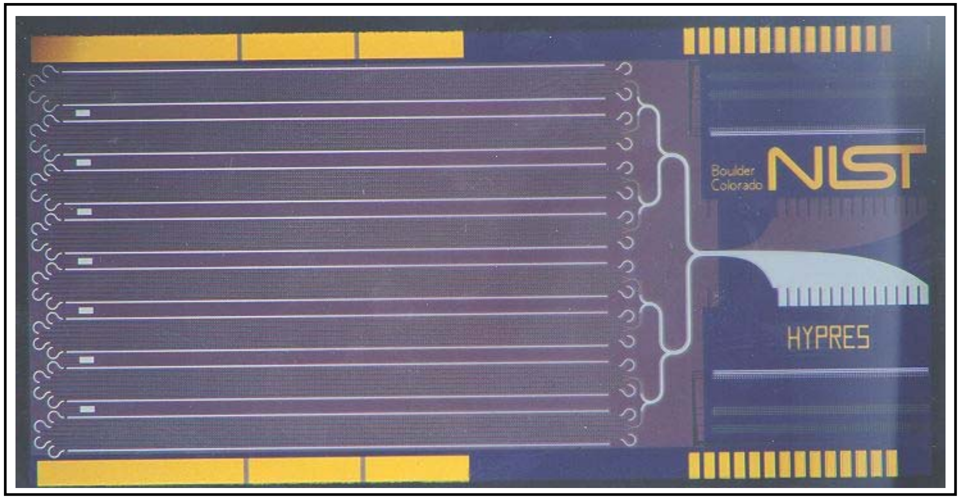
Brings the Power of Digital Processing to the RF Domain and changes the Paradigm of Wireless Communications

SME = Superconductor Micro-Electronics

HYPRES

Quantum Accuracy

Commercial Primary Voltage Standard for Metrology



1cm x 2 cm 10 Volt Chip with
5ppb accuracy
(23,000 Josephson junctions)

Cryocooled Voltage Standard System

This application cannot be done using any other technology...

HYPRES

Ultra-High Sensitivity

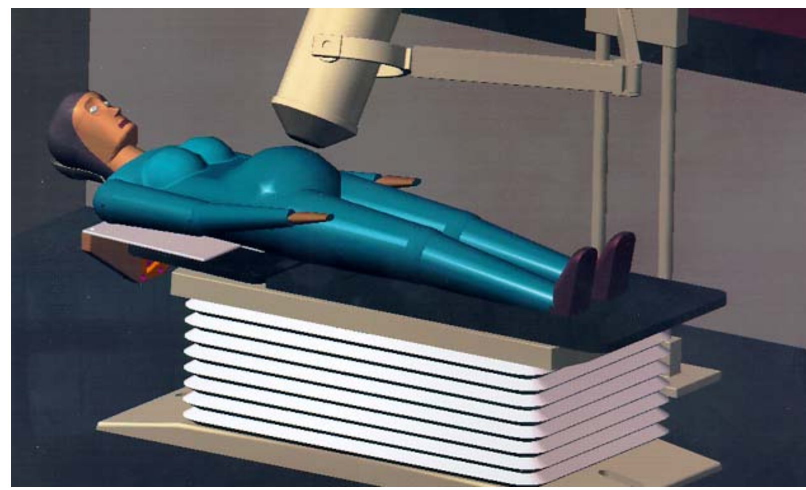
Examples of Commercial SQUID-based Magnetometers

(SQUID - Superconducting QUantum Interference Device)

Magneto-Encephalogram (brain currents detection)

CTF MEG System

Fetal Magneto-Cardiogram (fetal heart currents detection)



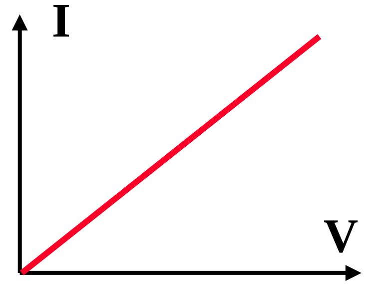
Hypres/BTi FMCG System

These applications cannot be done using any other technology...

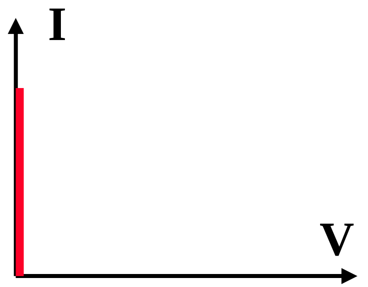
HYPRES

Superconductivity

Zero Resistance

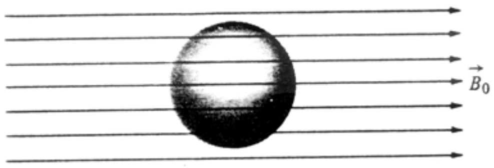


T > Tc



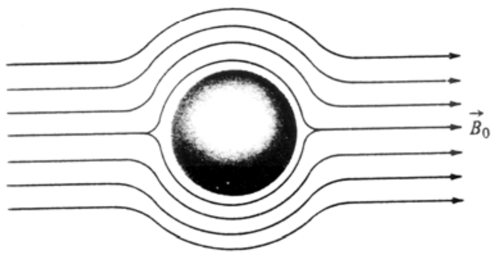
T < Tc

Expulsion and Quantization of Magnetic Flux



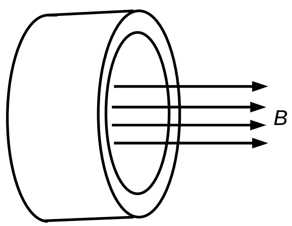
T > Tc

(AT ROOM TEMPERATURE)



T < Tc

(IN CRYOCOOLER)



T < Tc

$$\Phi = \int B_n dA = n\,\Phi_0$$

$$\Phi_0 = h/2e = 2.07 \text{ mV}\cdot\text{ps}$$

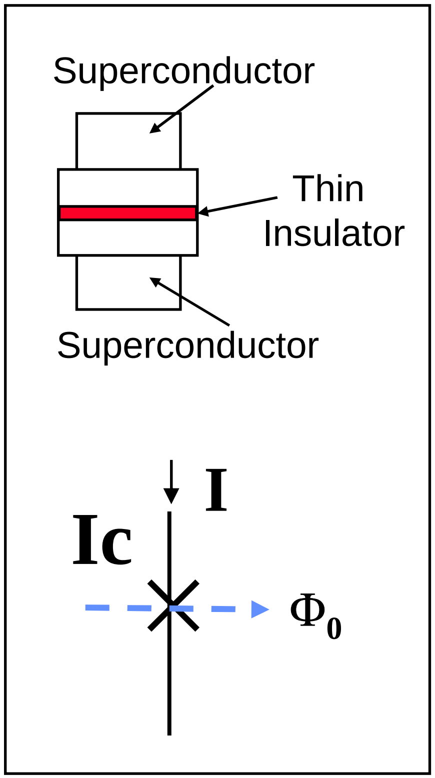
$$= 2.07 \times 10^{-15} \text{ Wb}$$

Single Flux Quantum (SFQ)

HYPRES

Josephson Junction Devices

Active component (switch) in superconductor electronics



Josephson Junction

I < Ic

JJ stays superconductive

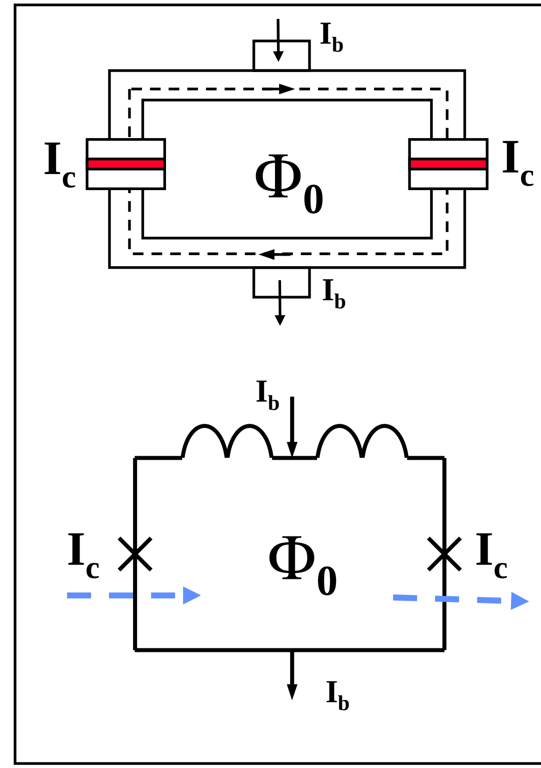
$$I = I_c \sin(\phi)$$

I > Ic

JJ goes resistive and passes magnetic flux through

$$\tau = \Phi_0 / Vc$$

Typical Critical Current:
Ic ~ 0.1 mA
Time constant :
τ ~ 1 ps (3-µm process)
τ ~ 0.1 ps (0.2-µm process)

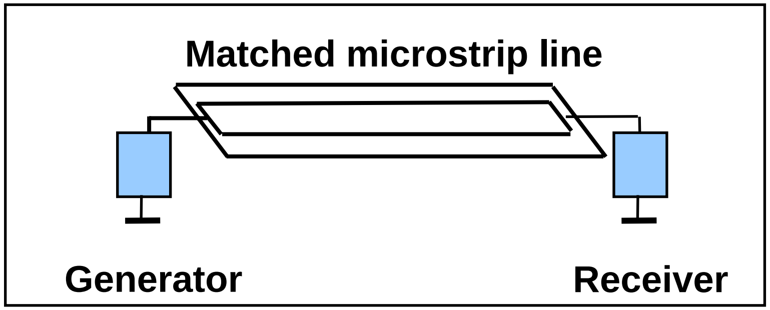


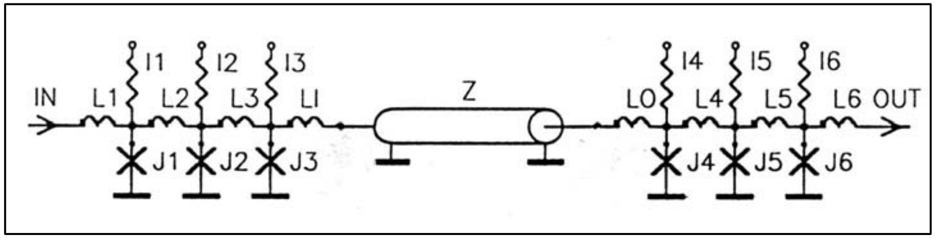
Memory cell

HYPRES

Superconductive Transmission Lines

Microstrip Lines can ballistically transfer picosecond waveforms



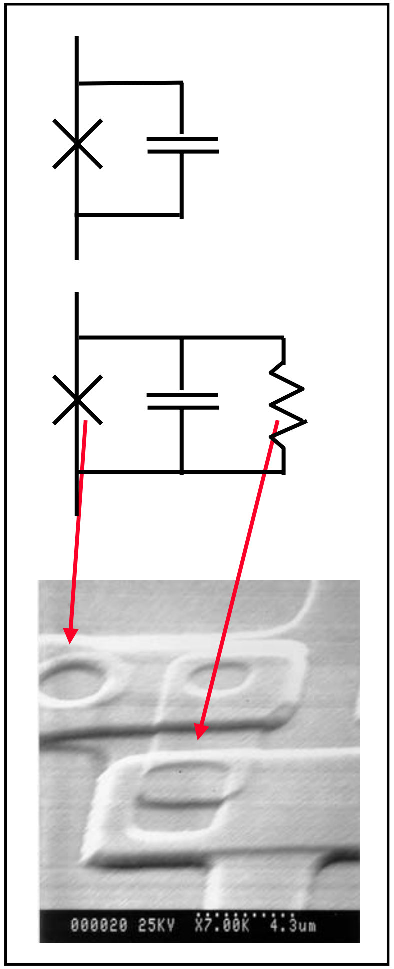


- **Semiconductor VLSI speed is limited by interconnect delays (RC-type charging)**
- **Superconductors have unique capability to transfer picosecond waveforms without distortions with speed approaching speed of light**
- **Crosstalk between neighboring transmission lines is very small**
- **Josephson junction impedance can be matched to that of microstrip lines**

HYPRES

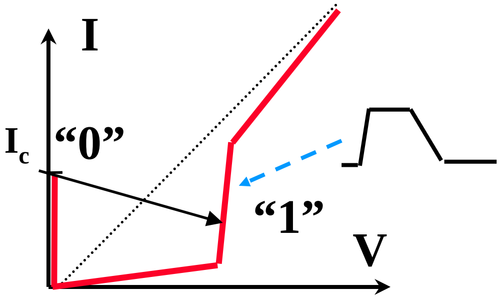
Josephson Junction Behavior

Picosecond waveforms and time responses



70-80's

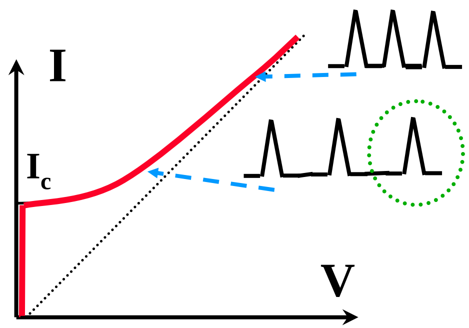
Latching logic



Voltage pulses
(picosecond front, nanosecond tail)

90's

RSFQ Logic



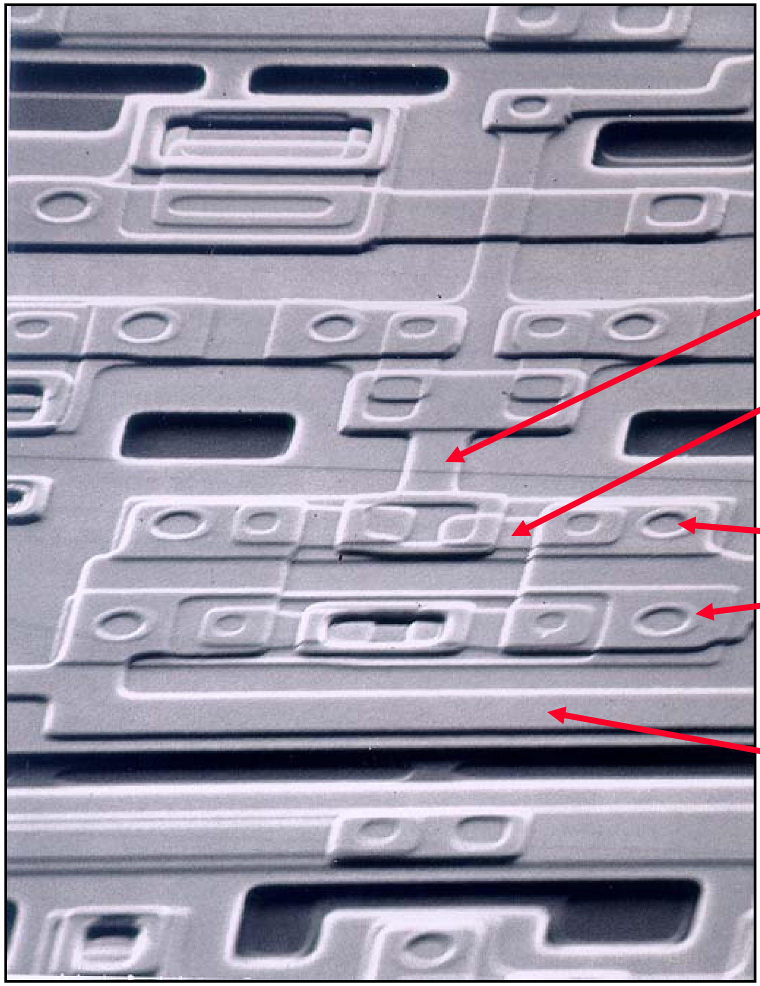
SFQ pulses with quantized areas
(picosecond front and tail)

$$\int V dt = \Phi_0$$

Adding a shunt resistor allows the generation of separate SFQ pulses

HYPRES

RSFQ Gate Physical Layout on IC



Toggle Flip-Flop Layout

Non-storage Inductance (~6 pH)

Junction Shunt (~1 Ω)

Junctions of different area (min. area = 3 µm x 3 µm)

Storage Inductance (~12 pH)

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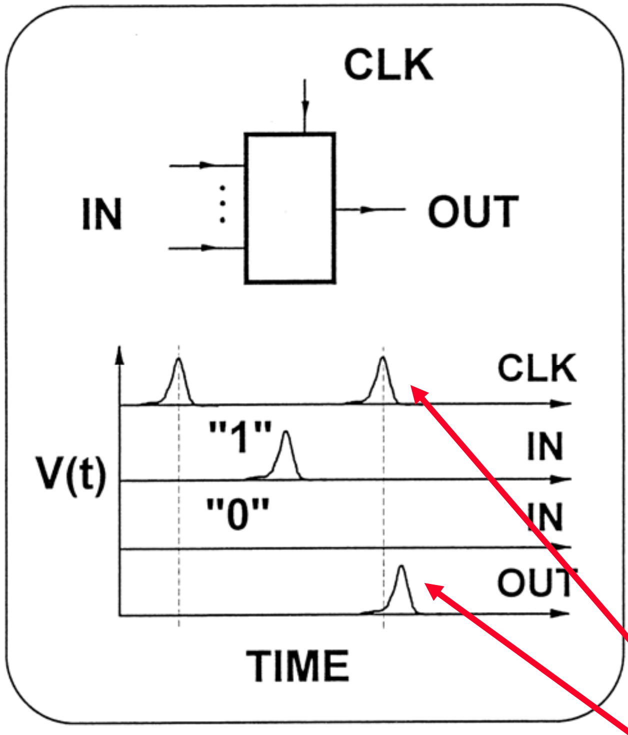
RSFQ Basic Convention

***RSFQ** - Rapid Single Flux Quantum*

Logic “1” - presence of a data SFQ pulse between two clock SFQ pulses

Logic “0” - absence of a data SFQ pulse between two clock SFQ pulses



Both Data and Clock are SFQ voltage pulses V(t) with quantized areas

$$\int V dt = \Phi_0 = h/2e = 2.07 \text{ mV} \cdot \text{ps}$$

SFQ pulses

Synchronous pulse coding of information

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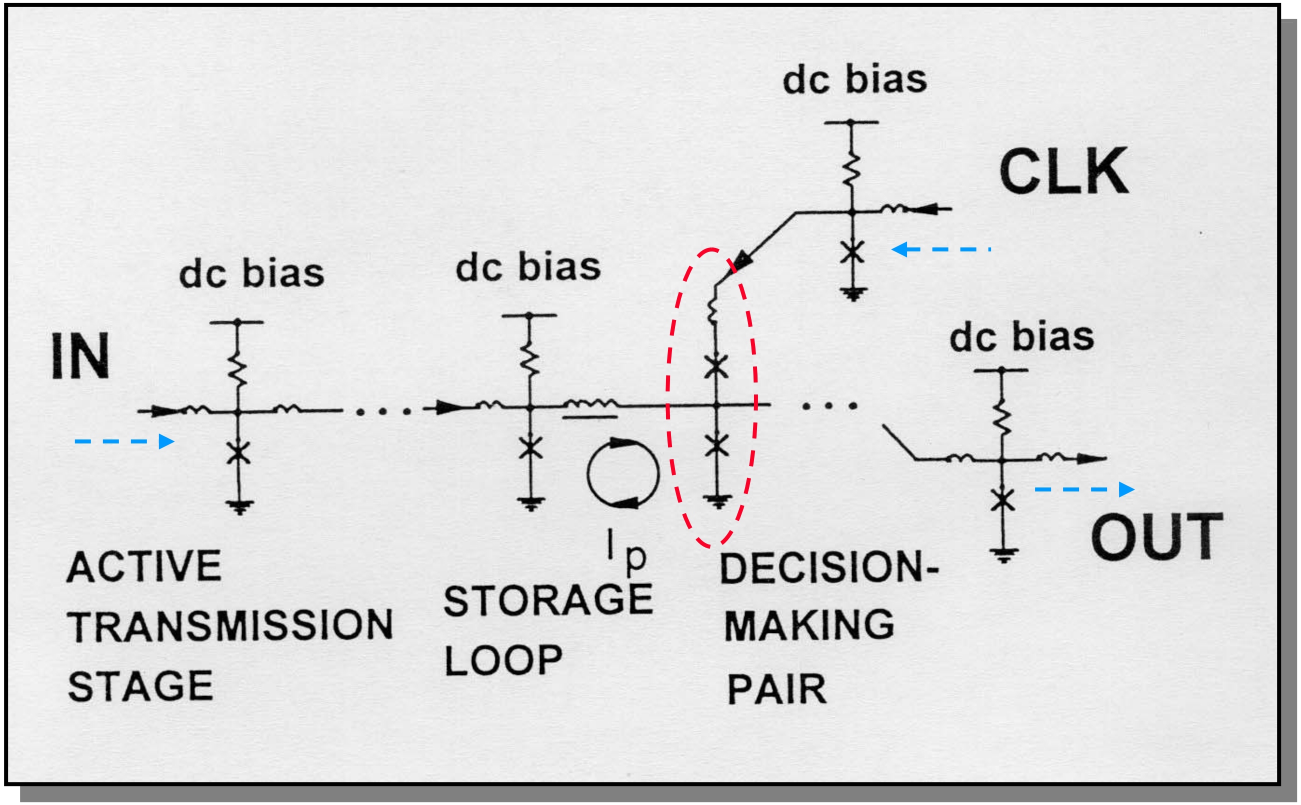
RSFQ Logic - Basic Components

How to generate, transfer, store, and switch SFQ pulses



Non-storage inductance ~ 6 pH vs. Storage inductance ~ 12 pH

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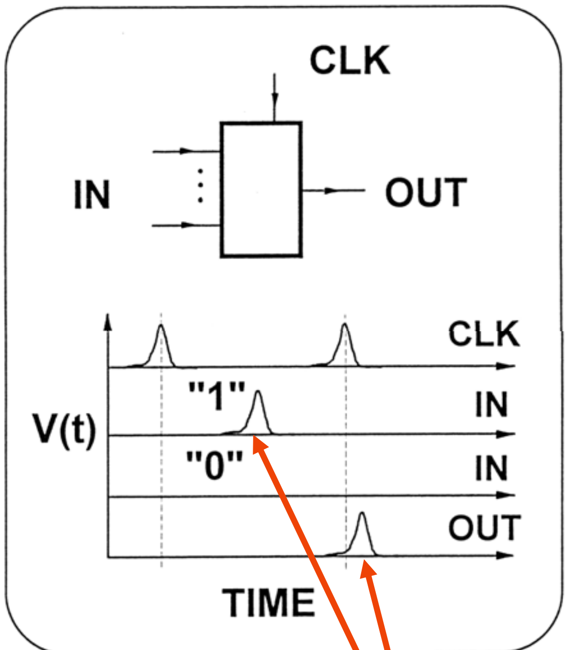
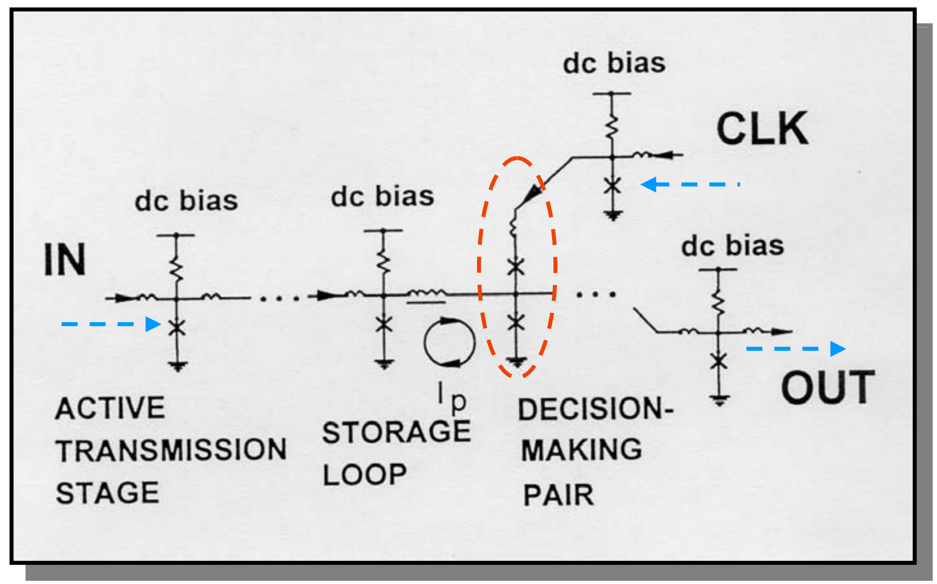
Rapid Single Flux Quantum (RSFQ) Logic

Both Data and Clock are SFQ voltage pulses V(t) with quantized areas



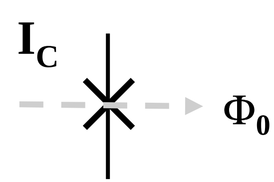
$$\int V dt = \Phi_0 = h/2e = 2.07 \text{ mV}\cdot\text{ps}$$



Synchronous pulse coding of information

SFQ pulses

Typical Critical Current:
Ic ~ 0.1 mA
Time constant :
τ ~ 1 ps (3-μm process)
τ ~ 0.1 ps (0.2-μm process)



Josephson Junction

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Why RSFQ Logic ?

	Latching logic	RSFQ logic
Data Presentation	Voltage	Magnetic flux
Natural quantization	No	Yes ($\Phi_0 = h/2e$)
Power consumption	~ 3 pW/gate	~ 0.3 pW/gate
Power supply	AC	DC
Self-timing possible	No	Yes
Maximum IC Speed	~ 3 GHz	~ 300 GHz

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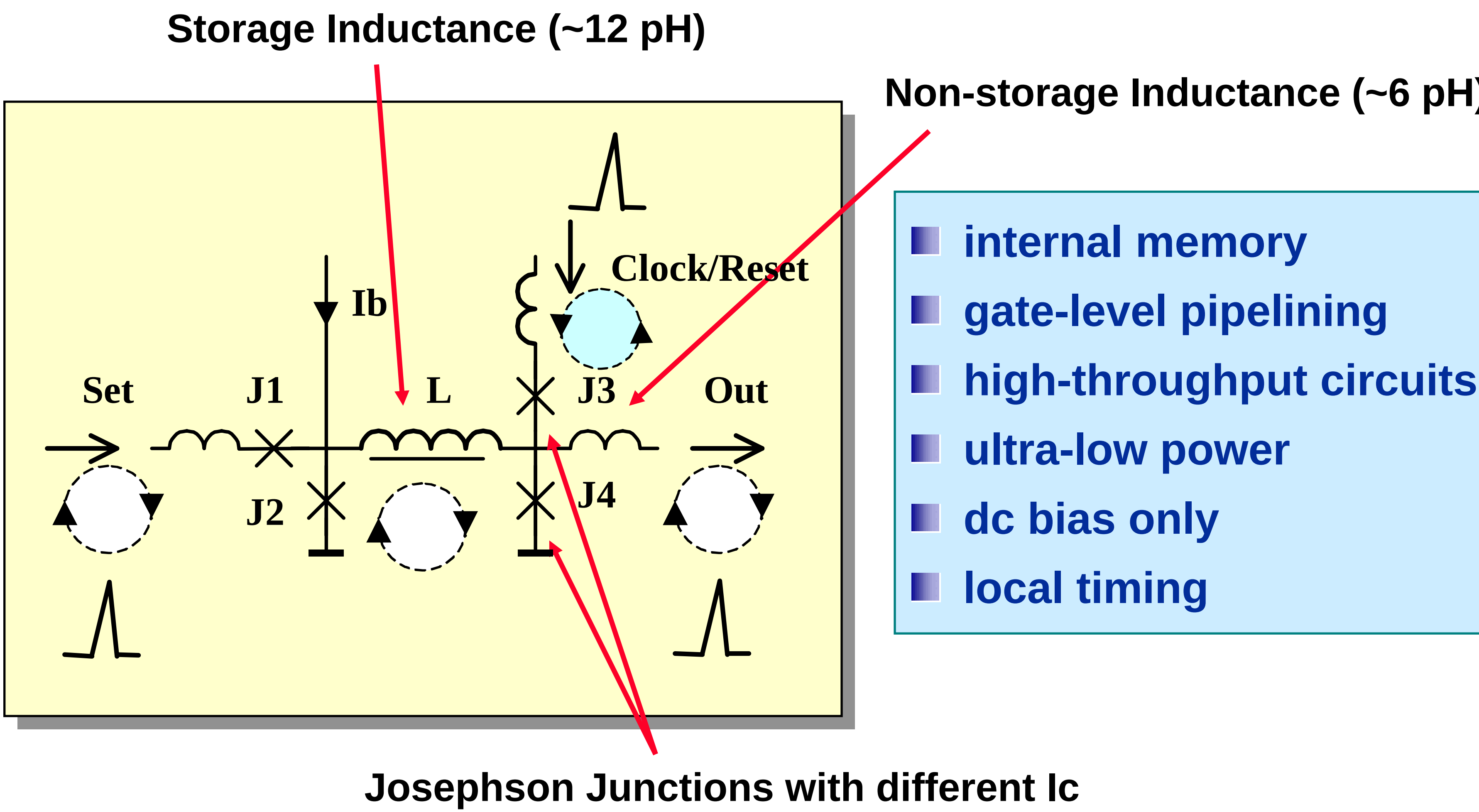
RSFQ Logic Gate: RS Flip-Flop



- internal memory
- gate-level pipelining
- high-throughput circuits
- ultra-low power
- dc bias only
- local timing

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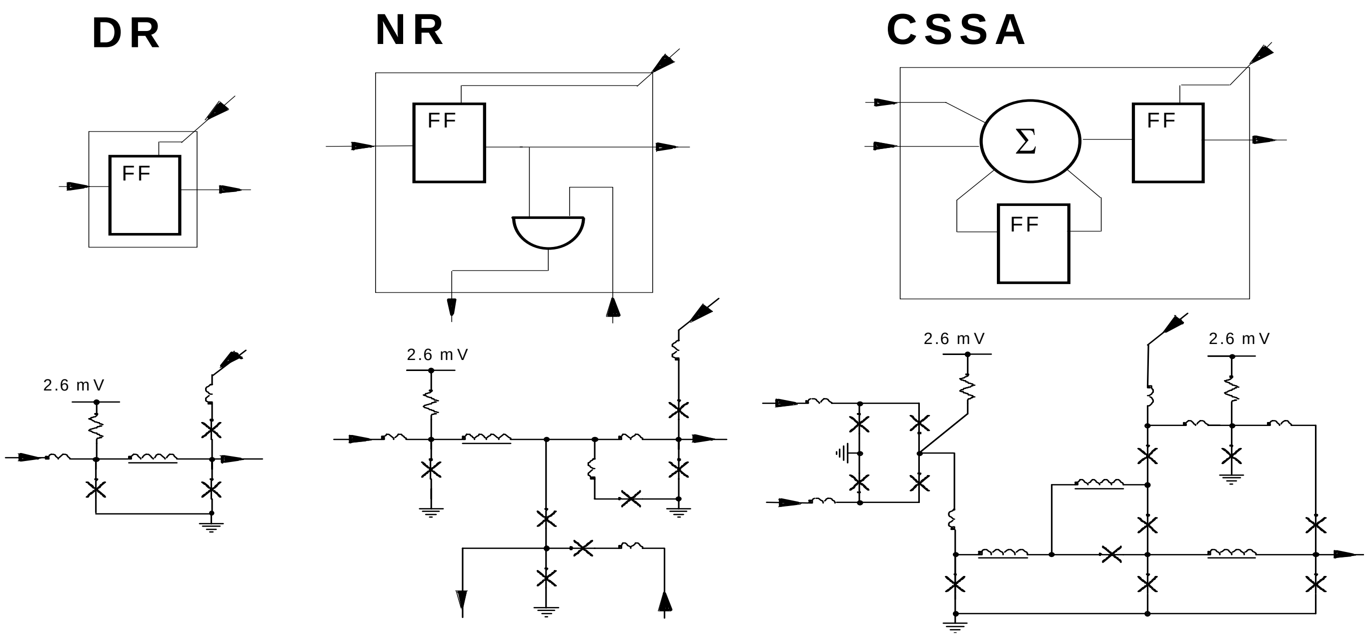
RSFQ Gates - Natural Flip-Flops

Basic Set of RSFQ Elementary Cells



D flip-flop

D flip-flop
with AND

Carry-Save
Serial Adder

T flip-flops, RS flip-flops, and their modifications with DRO/NDRO

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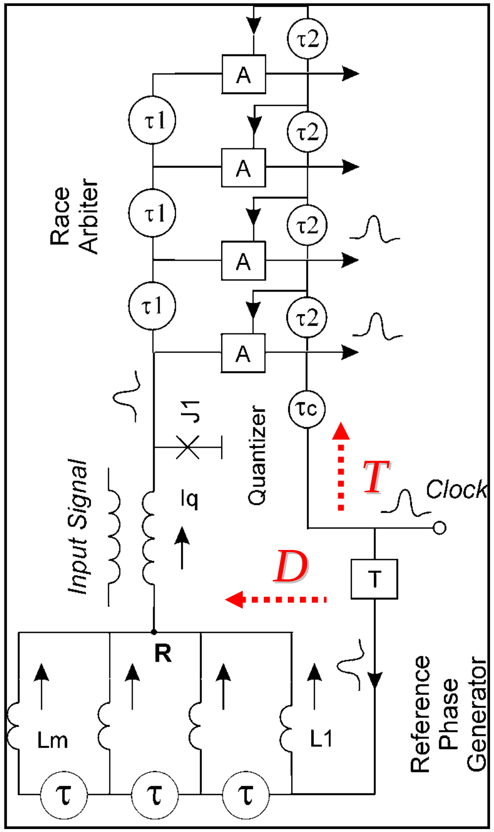
ADC Front-End Design

Phase (Time Delay) Modulation-Demodulation Architecture



Accurate measurement of time delays modulated by input signal

- **Modulation:**
  - **Clock generates two identical SFQ pulse trains (*D* goes via Quantizer, *T* goes via a delay)**
  - **Input signal induces additional current in the Quantizer**
  - **This additional current changes time of releasing SFQs of train *D* from the quantizer**
- **Demodulation:**
  - ***T* and *D* SFQ pulse trains meet at the synchronizer (race arbiter)**
  - **change in arrival time of train *D* vs. train *T* is measured in synchronizer**

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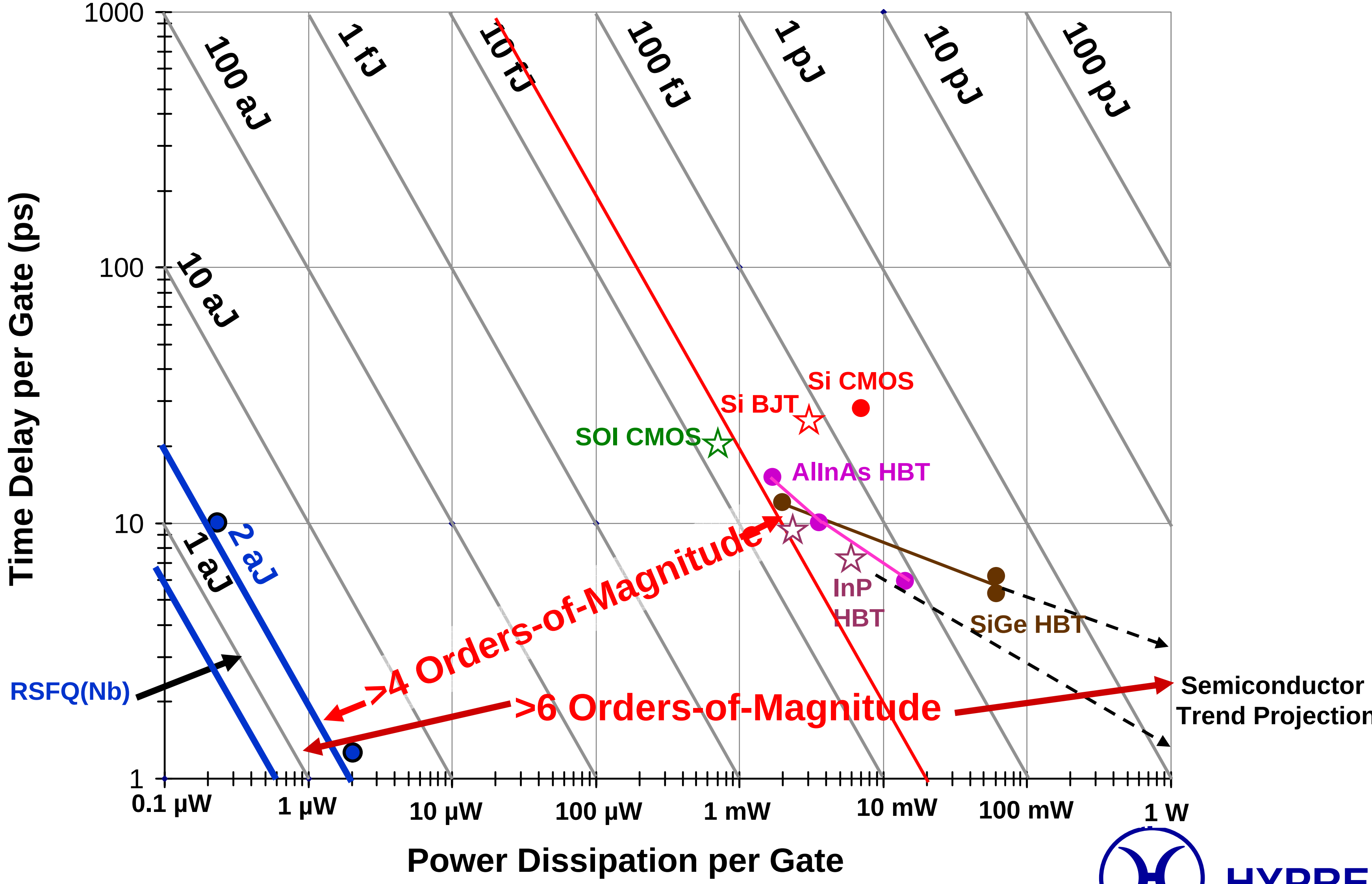
Performance Metric: Power-Delay Product



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HYPRES Commercial Nb Foundry

MAG Metal Deposition System

1988

High-J_c Trilayer Deposition

1997

6" Wafer Dicer

1998

Chem.-Mech. Polisher

1999

6" Coat & Develop Track

2001

0.8-µm Projection Aligner

2001

Major Fabrication Facility Upgrade in 2003-2004

PECVD Oxide Deposition

2003

Oxide Etching System

2003

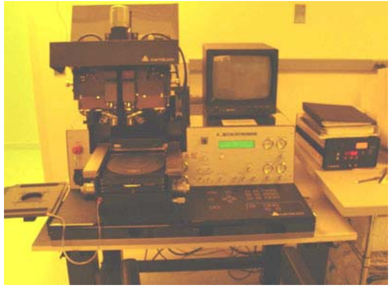
Metal Etching System

2003

E-beam Metal Deposition

2003

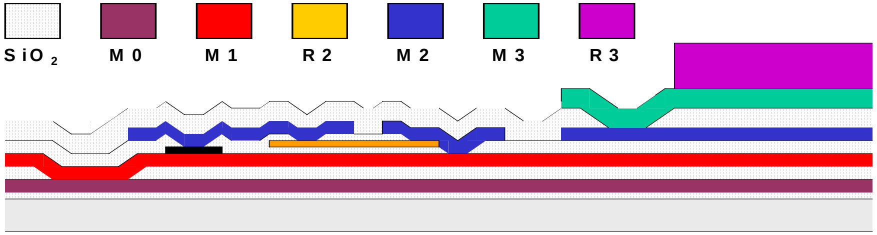
1.0-µm Contact Aligner



2003

Flip-Chip MCM Bonder

2004



4 Nb (superconductor) metal layers
2 resistor layers
1 Nb-AlO-Nb Josephson junction trilayer

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HYPRES, Inc. - Company Information

- Founded in 1983, HYPRES is a complete superconductor electronics company, offering design development, fabrication, testing, and packaging in a commercial production environment
  - Privately-held Small Business in Elmsford, NY, located 30 miles north of New York City
  - Team of 40 (mostly advanced degreed)
  - 16,000 sq. ft. facility includes commercial Nb foundry
- HYPRES is the premier commercial supplier of Primary Voltage Standard circuits and systems worldwide
- HYPRES commercial Nb Foundry has 8-10 mask releases per year and offers individual chip sites at only $80/mm^2

For more information visit http://www.hypres.com

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