JTRS FREQUENCY EXTENSION BEYOND 2GHZ AND SATCOM-ON-THE-MOVE (SOTM) USING SUPERCONDUCTOR MICROELECTRONICS -- *A QUANTUM LEAP IN PERFORMANCE*

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ABSTRACT

Superconductor MicroElectronics (**SME**) enables the realization of the true **Digital-RF** architecture, extending the flexibility and fidelity of digital processing up to multi-GHz speeds. HYPRES is developing **Digital-RF** subsystems that provide wideband and narrowband OBJECTIVE-level performance for WIN-T, FCS, TCA and JTRS communications systems. These subsystems are designed for near-term insertion into existing and future systems providing dramatic performance improvements and major reductions in SWaP and life cycle cost. This quantum electronics technology provides a quantum leap in performance -- bypassing the slow incremental improvements of traditional mostly analog electronics – to revolutionize future RF systems. This revolutionary SME technology provides unparalleled accuracies, spectral purities and ultra fast speeds that are otherwise unattainable with competing semiconductor technologies.

The advantages and features of SME technology can be applied to a wide range of Military satellite communications applications to include an extended family of JTRS SCA compliant radios in the 2 GHz to 55 GHz band and Digital Beam-Forming (DBF) Phased Arrays that make SATCOM-On-The-Move (SOTM) viable.

1. EXTENDING JTRS SCA BEYOND 2 GHZ

SME technology, with its unique combination of features, significantly enhances the feasibility of realizing a family of multi-mode, multi-band, programmable SATCOM radio systems based on a common architecture, such as the SCA, that extends JTRS from 2 GHz to 55 GHz. SME features ultra fast mixed signal (analog and digital) circuits with extremely low power dissipation that are naturally radiation hardened. Moreover, this cryogenic low-noise technology also features one of the most sensitive energy detectors. Together, these features lead to a collection of multi-GHz circuits – high-fidelity broadband data converters, ultra low-jitter clock sources, ultra-fast digital logic and memory elements – which enable a new **Digital-RF** radio architecture. Some of the benefits of the HYPRES **Digital-RF** approach for MILSATCOM include:

Much higher G/T allows more traffic with a smaller antenna. Improvements of 3 to 6 dB for fixed and transportable reflector antenna systems are feasible due to the ultra low noise temperature of the superconducting RF front end. This allows much higher information throughputs and/or diameter reductions of 30-50% (and more for phased arrays, see SOTM section).

Satellite throughput is more than doubled through the use of higher-level modulation techniques. Correlation-based **Digital-RF** receivers greatly improve S/N ratios allowing the use of higher-level modulation techniques that substantially increase capacity ("bits per hertz").

Linearization of near-saturated HPAs allows lower power, less expensive transmitters. HPAs may be operated well into their non-linear region providing typical improvements of 3 to 6 dB through the use of real time dynamic pre-distortion adjustments and HPA output feedback that yields power amplifiers smaller in size and power, and able to readily accommodate wideband multi-carrier operation.

All digital SME is inherently more robust (no temperature drifts, no temperature-sensitive oscillators or synthesizers, no bias & tuning adjustments). Spectrally pure digital converters replace thermal and spurious noise generating analog up and down converters. In addition, SME has a very high radiation hardness (orders of magnitude greater than hardened semiconductors) and does not exhibit microphonics.

Significant reductions in Size, Weight and Power (SWaP). A single product design eliminates requirements for multiple equipment units. **Digital-RF** eliminates analog LNA, RF to IF converters, combiners & dividers, as well as coaxial cabling and other components (even modems). It becomes feasible to install most of the electronics at the hub of the antenna, requiring only baseband and power cabling to the antenna – improving performance and reducing the cost and time-line of installation.

Enables the true software digital radio that provides OBJECTIVE JTRS Software Communications Architecture (SCA) compliant performance. A **Digital-RF** product can be programmed with the proper waveforms, frequencies & controls across the entire MILSATCOM space segment from UFO & UFO/E to Milstar, DSCS, GBS and commercial SATCOM. It is future proof and readily expandable to meet future communications needs such as MUOS, AEHF, WGS, AWS and TSAT.

Vastly Improved reliability and maintainability. Ultra high reliability, approaching MTBFs of 100 years, are obtainable. There is a huge reduction in maintenance and logistics requirements as a very small number of platforms with common components can address the broad range of MILSATCOM needs. Operations complexity is reduced with a common user interface and SATCOM terminal design configurations are simplified. For example, a single digital radio and analog HPA eliminates separate up and down converters, modem, and LNA. The all digital, software programmable architecture creates a single universal platform that can be configured dynamically and/or periodically to suit many different services.

HYPRES is currently developing SME components for a JTRS compliant **Digital-RF** transceiver operating up to 2 GHz. Our current generation of SME is capable of extending digital processing up to about 10 – 12 GHz. The **Digital-RF** architecture provides direct conversion of broadband RF signals to digital format, enabled by ultra-fast, quantum-accurate, analog-to-digital and digital-to-analog converters (ADCs and DACs), and ultra-fast digital signal processing electronics. In this architecture, non-linear frequency-specific analog components, such as analog mixers and channelizers, are replaced with their high fidelity, software reconfigurable digital counterparts, producing a true software radio.

A block diagram of the **Digital-RF** transceiver is shown in Figure 1. In the receiver, the RF signal from the antenna is filtered and sent directly to an ultra low noise bandpass ADC, without first down converting using an analog mixer and local oscillator. Down-conversion is accomplished completely in the digital domain, where it is easily reprogrammed. Even the (digital) local oscillator is built within the SME architecture. A digital decimation filter is used to decrease the down converted output bandwidth, while increasing the effective number of bits. While normally a quadrature receiver, only one channel is shown for simplicity. There may also be channelization into multiple baseband channels using loss-less digital copies from the ADC. Finally, with only slight modifications, the receiver can be reconfigured as a correlation-based receiver, using a digitally generated template and an appropriately matched digital filter.

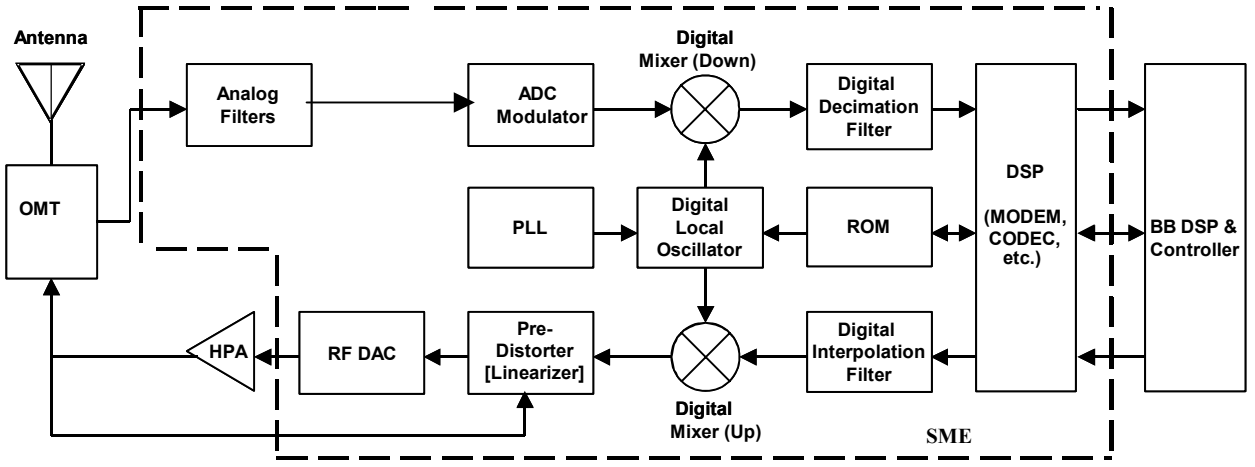

Figure 1 A Direct Digital Frequency Conversion Transceiver Architecture

When the waveform of the signal of interest is known, it becomes possible to use a matched filter based on correlation to perform digital filtering in the **frequency and time domains simultaneously**. This is considered the optimum matched filter. Such a correlation filter will process out all noise that is not correlated. Signal power remains unchanged while noise power decreases in the correlation process. Other signals that the correlator is not programmed to correlate are similarly decreased in a noise-like manner.

HYPRES technology brings the ultimate matched filter to communication systems. Prior to the advancement of HYPRES technology, RF correlation-based receivers were not possible for real time communication systems because the "solution space" was too large for conventional semiconductor-based technologies. The difference in processing time is in the microsecond range for HYPRES technology (very acceptable for communication systems) vs. minutes/hours for conventional semiconductor-based technologies. S/N improvements of 20 to 40 dB are achievable for the widest MILSATCOM bandwidths.

The transmitter carries out the same digital functions in reverse, with a fast DAC reconstructing the RF signal directly, just before the high-power amplifier (HPA). The diagram also shows a pre-distortion module, a dynamic digital equalizer that is combined with the DAC to compensate for non-linearities in the HPA. Also, multiple channels can be combined digitally into one broadband **Digital-RF** signal before amplification, requiring only a single HPA.

2. SATCOM-ON-THE-MOVE (SOTM) USING PHASED ARRAYS

HYPRES SME technology enables WIN-T wideband Phased Array Digital Beam Forming (DBF) hardware for narrow-beam satellite communications, with performance significantly exceeding that of any current or projected system using conventional RF technologies. Current phased arrays are limited by the performance of conventional analog approaches that include the implementation of beam steering by coarse, element phase shift adjustments. However, the speed, performance and cost effectiveness of SME technology makes SOTM feasible and practical.

The wideband DBF subsystem is based on high-performance ADCs and DSP hardware with True Time Delay (TTD) adjustments providing high resolution, precise, frequency independent beam forming. The very low noise temperature of the integrated superconducting ADC and the increased gain due to much finer element phase adjustments significantly enhances the signal-to-noise ratio of the receiver. In addition, the signal-to-noise ratio is dramatically increased with HYPRES correlation based receiver techniques. Some of the benefits of using HYPRES SME technology for SOTM phased arrays include:

Array size is reduced by 75 - 85% due to improved G/T (6 to 8 dB through improved gain and reduced noise temperature). These much smaller arrays require much lower numbers of elements, resulting in dramatically lower costs. The resulting arrays require only 15 to 25% of the "real estate" on a target platform simplifying integration and lowering the overall profile.

HYPRES DBF Arrays with correlation-based receivers provide highly enhanced throughput (increased capacity) and/or immunity to LOS blockage and foliage attenuation and/or increased anti-jamming capabilities. HYPRES correlation-based receivers provide dramatic signal to noise (Eb/No) improvements of 20 - 40 dB resulting in increased link margins that can be used to increase capacity and/or to "punch thru" the attenuation of partial blockages from foliage and structures and/or to increase immunity to jammers. Improved link margins also maintain time tracking in fading conditions.

Power Amplifier linearization and enhanced transmit gain (similar to receive antenna gain) provide similar overall gains for the transmit side to balance the link. Each individual element PA is operated well into its non-linear region providing typical improvements of up to 3 - 6 dB through the use of real time dynamic pre-distortion adjustments. This yields power amplifiers with smaller size and power consumption, and the ability to readily accommodate multi-carrier operation. This can be done very cost effectively using the HYPRES SME IC pre-distorters in each element.

Deep nulls and increased SNR provide enhanced jammer reduction. The improved beam focus due to frequency independent, higher resolution beam phase alignments ($< 3^0$ at X-band with HYPRES TTD phasors vs. 45^0 - 90^0 using analog techniques) provides greatly improved rejection of interference with adaptive pattern nulling. Nulls of up to 60 dB for active jamming reduction are obtainable. This also reduces quantization lobes for decreased antenna sidelobes and increased antenna efficiency. The result is better pointing resolution and improved transmit and receive gain. In addition, these significantly smaller arrays feature wider beamwidths providing additional

SNR improvements from less stringent tracking requirements.

HYPRES DBF provides low cost per element. Phased Array Element cost in the $100/element range is achievable with volume production. Overall array costs are reduced 75 - 85% due to G/T improvements that afford smaller arrays as described above. The combined benefits of smaller arrays and lower element costs provide dramatic overall recurring cost savings – an order of magnitude lower than conventional technology.

Life Cycle Costs are reduced using highly reliable, low maintenance DBF techniques. Ultra high reliability, approaching MTBFs of 100 years, are obtainable and communication system integration is easier and less costly due to all-digital configurations.

Multiple beam operation is achievable and affordable using ultra-high speed time division multiplexing with the same generic hardware. This allows simultaneous access to multiple satellites for increased communications flexibility and capacity as well as alternative routing in the face of blockages.

A block diagram of the basic SME Digital Beam Forming array element is shown in Figure 2. The beam forming process takes multiple signals from a spatial array of antenna elements, shifts their phased until they are coherent, and then combines them into a single signal corresponding to a beam wave front. Similarly, multiple beams can be formed from the same ADC sample using digital, loss less copies of the aperture signal applied to duplicate TTD and weighting networks.

The key to enabling wideband beam-steering capability is high data-rate signal processing to combine data between antenna elements. The HYPRES SME approach uses a superconductive circuit technology with a unique architecture to provide precise true time delay adjustments down to <1 picosecond resolution. The use of very high clock rates and other SME features enable very short controllable time delays that yield narrow beams with low side-lobes and higher efficiency in wide frequency bands. Weighting is provided for beam shaping and/or adaptive pattern nulling for interference rejection. Resolution is improved and gain is increased with the much more accurately synthesized beam wave front. True Time Delay beam alignment is frequency independent so that a wideband signal or multiple carriers are processed with the same accuracy. The HYPRES DBF system exhibits much better signal/noise ratios (SNRs), lower sidelobes and improved antenna efficiencies and beam pointing accuracies over traditional analog systems.

The technique utilizes over sampling analog/digital conversion and is followed by very-high-speed digital signal processing (DSP). The module architecture includes direct analog-to-digital conversion, a digital down-converter and a digital filter to deliver in-phase and quadrature (I & Q) Nyquist-rate digital baseband data.

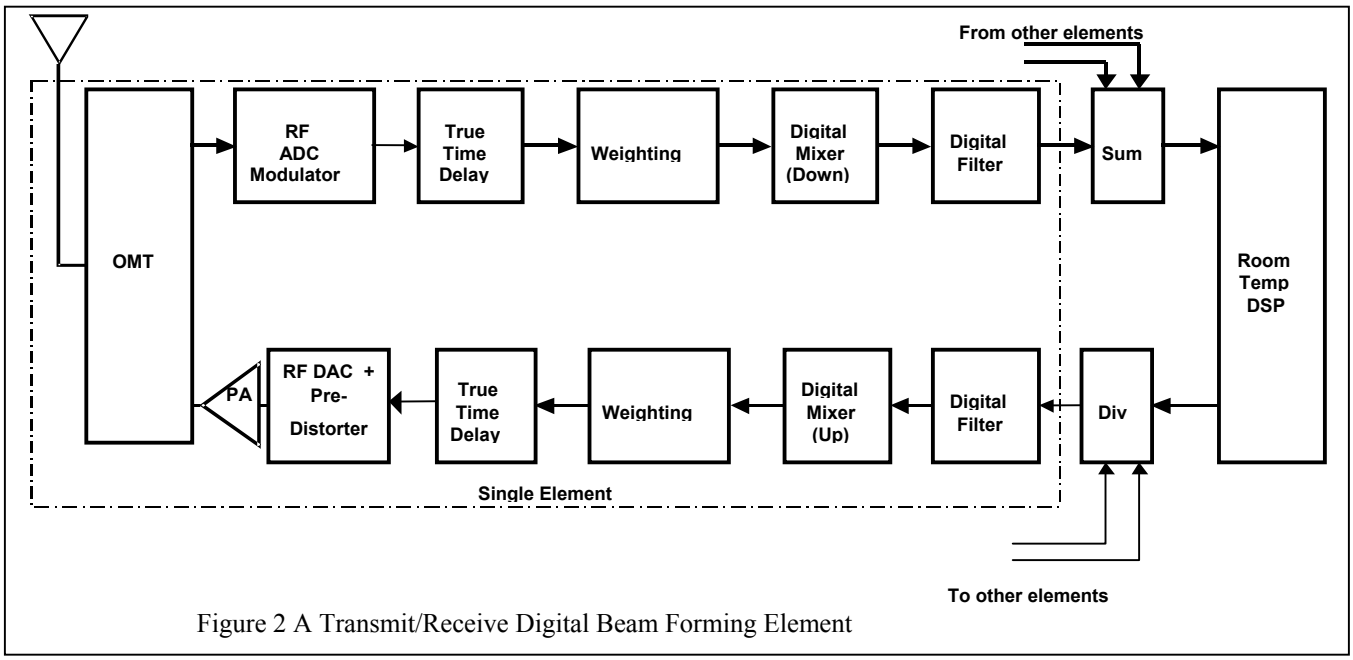

Figure 2 A Transmit/Receive Digital Beam Forming Element

On the transmit side, similar functionality provides transmit beam forming. A predistorter is included for each element to linearize each individual PA for near-saturation operation.

3. RSFQ- THE TECHNOLOGY BEHIND DIGITAL-RF

Extension of the JTRS SCA beyond 2 GHz and implementation of cost effective SOTM requires new state-of-the-art electronics technology. To enable this wideband digital "software radio" architecture, the RF hardware must avoid non-linear, frequency- and protocol-specific analog components that compromise interoperability and agility. On the transmit side, the waveform should be spectrally pure with as little intermodulation distortion as possible. This requires low noise, linear electronics for the entire transmit chain, including digital-to-analog converters and high power amplifiers. Similarly, a low-noise front-end is required on the receive side with a linear broadband analog-to-digital converters. By virtue of a unique combination of highly desirable properties, superconductor Rapid Single Flux Quantum (RSFQ) electronics technology is the enabling hardware technology for such advanced communication systems.

Superconductor rapid single flux quantum (RSFQ) electronics have the unique distinction of being the highest speed integrated circuit technology and also consume the lowest energy -- 1attoJoule ($=10^{-18}$J) per digital operation. RSFQ gates (toggle flip-flop) have been demonstrated above 750 GHz. RSFQ has been shown to operate at up to 25 GHz at the LSI level, and is projected to extend up to 250 GHz in VLSI structures. Power dissipation of superconductor ICs is also very small, only about 1 mW per chip.

RSFQ integrated circuits are manufactured using standard semiconductor manufacturing equipment; however, it requires fewer mask layers and less complex depositions. The process relies on thin-film technology, rather than doping profiles. Basic functionality, such as flip-flops, shift registers and counters, has been demonstrated, at 144, 66 and 120 GHz respectively. More complex devices implemented at 10s of GHz have included 128-bit autocorrelator, serial multiplier, demultiplexer, full adder, 14-bit digital comb filter, and 1-kbit shift register. 14-bit high resolution ADCs and 18-bit DACs have also been implemented at HYPRES. Also, unlike other proposed multi-GHz technologies, RSFQ ICs are already at integration scales up to 20,000 junctions per chip. A superconductor ADC chip is shown in Figure 3.

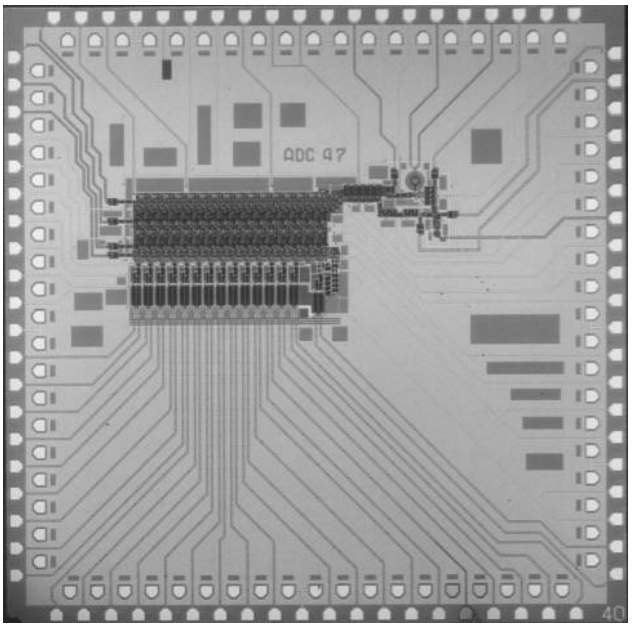

Figure 3 Superconductor ADC Chip

Superconductor RSFQ electronics facilitate the **Digital-RF** architecture, where the analog RF signal is converted to the digital domain directly behind the antenna and all signal processing is performed using software-controlled digital electronics. The front-end of the cryogenic superconductor **Digital-RF** receiver is a bandpass ADC, which contributes very little to the system noise temperature (T_s). The cryogenic operating temperature of RSFQ ICs (i.e., 4 to 5 degrees Kelvin) itself provides a 60 to 75 times reduction in the contribution of thermal noise compared to room temperature circuits. With this low-noise receiver, coupled directly to the antenna, the system noise temperature approaches the antenna noise temperature. For typical elevation angles of the antenna, the T_s is reduced by a factor of 2 - 4, depending on frequency, elevation angle, antenna design, etc. This is a 3 - 6 dB improvement in G/T. In addition, the ultra-low noise characteristic of the superconducting ADC is complimented by its extreme sensitivity that is orders of magnitude greater than conventional analog front ends. For example, sensitivities better than –150 dBm in a 1 MHz bandwidth are possible with SME.

4. EXTENSION OF DIGITAL-RF ARCHITECTURE BEYOND 2 GHZ

With the first generation of RSFQ superconducting electronics, characterized by a clock frequency of 20-25 GHz, this **Digital-RF** architecture has been extended to 6 GHz (about $1/4^{th}$ the clock frequency).

These first generation devices were fabricated with extremely conservative 3 micron lithography. HYPRES is developing second generation devices that increase clock speeds to 40 - 50 GHz, extending the direct conversion **Digital-RF** architecture up to 10 - 12 GHz.

The 40 - 50 GHz generation of SME, corresponding to device dimensions of 1.5 microns, is still well below the ultimate speed achievable with this technology. Scaling the devices results in a proportional increase in circuit speed up to the fundamental material limits. This limit for Nb is about 160-200 GHz for large-scale integrated circuits and about 800 GHz for single logic gates. In the next (3^{rd}) generation, scaling the devices down by a factor of two is expected to increase the clock speed up to 80-100 GHz, which corresponds to extension of the **Digital-RF** architecture to 20 - 25 GHz RF. The lithography requirement for even this 3rd generation is only 0.6 microns, which is rather modest compared to today's semiconductor lithography. Finally, shrinking the devices to about 0.3 microns will allow us to extend direct conversion to 40 - 50 GHz to the digital domain.

5. SUPERCONDUCTOR CIRCUIT COOLING

The huge leap in performance obtained with superconductor MicroElectronics (SME) is due to the fundamental physical properties of superconductors. These properties lead to unprecedented performance in integrated circuits, and to quantum accuracy in the digitization of high bandwidth analog signals. A key element in the packaging of SME products is the cryocooler -a cryogenic closed cycle refrigerator needed to maintain the superconductor IC at the low temperatures required for their operation. The technology for producing these cryocoolers has evolved over several decades, and recent developments now enable robust products with exceptional efficiency and reliability. Products utilizing superconductors for analog signal processing are already commercially deployed. Over 3000 units have demonstrated more than 11 million hours of operation with mean-time-between-failures (MTBF) exceeding 800,000 hours or over 90 years, an estimated uptime of 99.998%!

At the same time, the technology and product development roadmap is well established for packaging of superconductor digital circuits. Moreover, because of extremely low power dissipation, it is possible to provide thermal conditioning for several SME chips such as multiple ADCs, digital processing circuitry, and DACs with a *single* cryocooler. Therefore, RSFQ-based multi-channel software radios can be ***much smaller*** than conventional systems. Appropriate cryocoolers serving the varying requirements of civilian, military, and space markets have been defined with multiple available sources and technologies.

Cryocoolers are essentially refrigerators, where the term "Cryo" refers to reaching a temperature range typically below 100 Kelvin (K), and in the HYPRES SME case, around 5 K. In the superconducting electronics context, the cryocooler provides "thermal conditioning" of the circuits, much like other thermal conditioning methods (fans or passive coolers, etc.) are used for other electronics technologies. However, unlike conventional electronics, the cooling is not used to "get the heat out;" it is used to get the superconductive effect. Cryocoolers are the enabling package for SME and determine the overall SWaP of the SME-based system.

6. CONCLUSIONS

Superconducting MicroElectronics technology brings revolutionary changes in the design and implementation of RF microwave electronics. For the first time, it becomes practical to implement high frequency RF functions in the digital domain – all accomplished with unheard of low-noise performance, unparalleled accuracies, extreme spectral purities and ultra-fast speeds otherwise unattainable with competing semiconductor technologies, analog or digital. These new **Digital-RF** "tools" lead directly to systems with much smaller antennas, increased capacities (over the same satellites) and flexibility, all at a fraction of the cost of current technologies.

The Joint Armed Forces have well over a 100 different terminal types, each requiring specially trained personnel for operations and maintenance (O&M). These O&M costs comprise over 50% of the MILSATCOM system life cycle cost. HYPRES SME-based **Digital-RF** subsystems for software defined radios can extend JTRS common designs and interfaces across all SATCOM platforms from 2 GHz to 55 GHz. These subsystems are fully scaleable to add or reduce functionality based on specific mission needs and easily upgraded with new functionality to meet future Objective Force communications requirements.

SME technology exceeds the criteria for vehicular, shipboard or airborne SOTM applications. This technology is directly applicable to radar phased arrays. The ultra-low noise bandpass ADC front end and correlation-based receivers can also be easily adapted to

fixed and transportable reflector antenna systems for improved G/T and SNR that result in smaller antennas, increased capacity and improved performance margins. The speed, performance and cost effectiveness of SME technology makes near-term OBJECTIVE SOTM performance feasible and practical.

7. ACKNOWLEDGEMENT

The authors gratefully acknowledge Alan Kadin, and Oleg Mukhanov of HYPRES for their contributions.

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