IDROMEL: AN OPEN PLATFORM ADRESSING ADVANCED SDR CHALLENGES

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ABSTRACT

This paper presents the ANR project IDROMel, which aims at developing reconfigurable SDR (Software Defined Radio) equipments. IDROMel is a 3 years project that started early 2005 and finishes at the end of year 2008. The main objective of IDROMel is to define, develop and validate a powerful SDR platform combining very last technology progresses. The platform includes software parts (reconfigurable protocol stacks) and hardware parts (a base band board and a Radio Frequency Front end, RF). Both parts are presented in this paper.

1. INTRODUCTION

IDROMel is a French RNRT project aiming at defining, developing and validating a powerful Software Defined Radio (SDR) [1][2] platform combining very last technology progresses such as:

- a completely flexible baseband processing,
- MAGALI Network on Chip based integration,
- FPGA partial reconfiguration support,
- very wide band RF from 200 MHz to 7.5 GHz agility,
- 4 x 4 MIMO support,
- flexible MAC design for vertical handover support.

The features of the platform permit to explore many SDR scenarios. The targeted scenario of the IDROMel project [3] is a vertical handover between a cellular UMTS-like waveform and an ad hoc OFDM waveform. Hence, the aim of our work is to enable a terminal to move seamlessly in a heterogeneous network, including at least two different RATs (with different QoS parameters, frequency bands and bandwidths). The selected RATs in the frame of IDROMel are UMTS and WiMax, but as far as possible the developed terminal will be able to deal with other RATs, thanks to its reconfigurability abilities.

Moreover, we target a quasi-optimal handover: optimality means that no degradation due to handover is observed. This quasi-optimal handover will be possible thanks to a Duplication and Merging approach developed in E^2R and Rhodos projects. The basic idea of this approach is to send the data flows from and to the mobile through 2 radio interfaces at the same time during the handover. In order to achieve this *soft handover*, there is a clear need of 2 RF front-ends and two entities of the protocol stacks working in parallel.

The global architecture (hardware and software) of the mobile equipment is designed in order to fulfill the following functionalities:

- working in real-time,
- including the necessary protocol stack that enable the communication with a base station or an Access Point,
- ability to communicate through 2 different RATs with 2 different bandwidths and frequency bands,
- reconfigurability of each RAT, including physical layer,
- ability to switch seamlessly from a RAT to another.

This paper details the main components of the IDROMel platform. An overview of the platform is given in Figure 1.

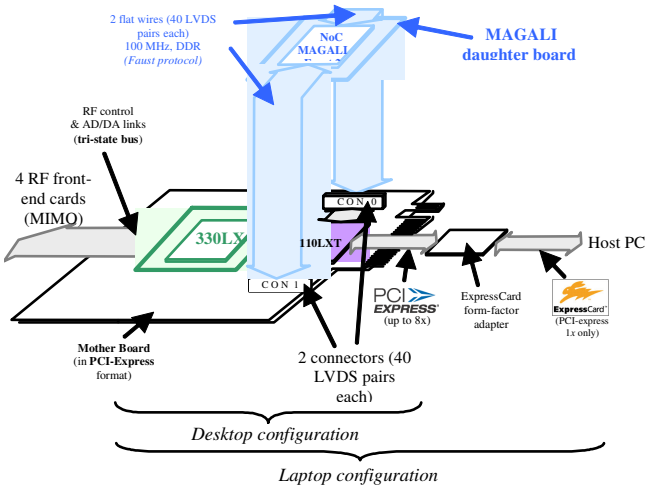

Figure 1 - Overview of IDROMEL system architecture

The paper is organized as follows. A part of the baseband processing as well as the management is implemented in a PCIExpress / ExpressCard compatible card. It is composed of a Virtex-5 330LX and a Virtex-5 110LXT. The Virtex-5 110LXT is mainly controlling the PHY layer part, as well as providing a convenient interface to the host PC running the MAC and upper layers of the two protocol stacks is depicted in part 2. The Virtex-5 330 implements a part of the digital baseband processing presented in part 3 and is able to support up to 4 RF chains as explained in part 4. The MAGALI NoC architecture is described in part 5. Many configurations are supported thanks to the parameterizable and reconfigurable approach of all processing units embedded in the NoC architecture. Part 6 explains how the Partial Reconfiguration (PR) of FPGA has also been integrated in the NoC network through the extension of the network into a Xilinx FPGA. This gives the capability to the system to evaluate and test this new feature of FPGA combining HW processing efficiency and SW flexibility. Details of the wide band RF architecture are given in part 7. Part 8 exposes the futuristic cognitive radio features that could also be supported by the IDROMel platform.

2. MAC AND UPPER LAYERS

The MAC and upper layers of the waveform protocol stacks run on a Linux RTAI host PC connected to the hardware platform. Each protocol stack has an IP interface on which application layers may be implemented. The corresponding C software is a set of RTAI modules.

The IDROMel target scenario is a quasi-optimal handover between two waveforms, optimality meaning that no degradation due to the handover is observed from the terminal user point of view. To achieve this, the basic idea of our approach is to send the data flows from and to the terminal through two radio interfaces at the same time during the handover phase: initially, on the terminal, only one of the two waveforms (ad hoc OFDM waveform or UMTS-like waveform) is running. Some measurements, coming from lower layers, like for instance a signal-to-noise ratio, are received by a scheduling entity responsible of the triggering of the handover process. This process begins with the installation of the second waveform on the terminal, in coexistence with the existing one - there is therefore a need of at least two RF front-ends and two complete protocol stacks running in parallel. Once the communication flow is operational on the second waveform, the first one is removed from the terminal and the handover process is completed. The resulted functional overall architecture is depicted in Figure 2.

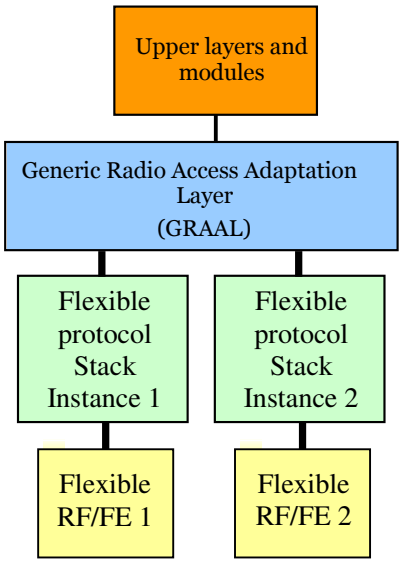

Figure 2 - Functional Architecture for a Double RAT Transmission

In this architecture, the GRAAL (Generic Radio Access Adaptation Layer) module aims at hiding the heterogeneity of the RATs (QoS parameters for example) to the upper layers. Moreover, the 2 instances of protocol stacks and Radio Frequency Front-End (RF/FE) allow the mobile terminal either to communicate through 2 different RATs during a vertical handover, either to communicate through one standard using multiple antennas processing (MIMO).
Therefore, in addition to the individual MAC and upper layer modules, a dedicated scheduling module has been specified, associated to cross-layer mechanisms allowing the handover triggering.

3. FPGA BASEBAND PROCESSING

The platform is planned to be pluggable to a laptop. It is driven by an embedded 32 bits micro-controller. The interface with the host PC is a 8x PCIExpress link. The baseband unit assembles 7 flexible processing units, each of them complemented with an 8 bits micro-controller and a DMA engine. These units are interconnected through an Advanced VCI crossbar interconnect. Several parallel and serial general purpose I/O modules are used to control the RF, interface with the AD/DA converters and to extend the system with daughter boards (e.g. a MAGALI chip). The 32 bits micro-controller is a Sparc V8 (LEON3, by Jiri Gaisler). It is responsible for the interface with the MAC layer, run on the host PC, and for the control of the DSP part. This global control unit is mapped in a dedicated FPGA (Virtex V LXT110 from Xilinx). The DSP part is mapped in a second, larger FPGA (Virtex V LX330). Figure 3 illustrates this architecture.

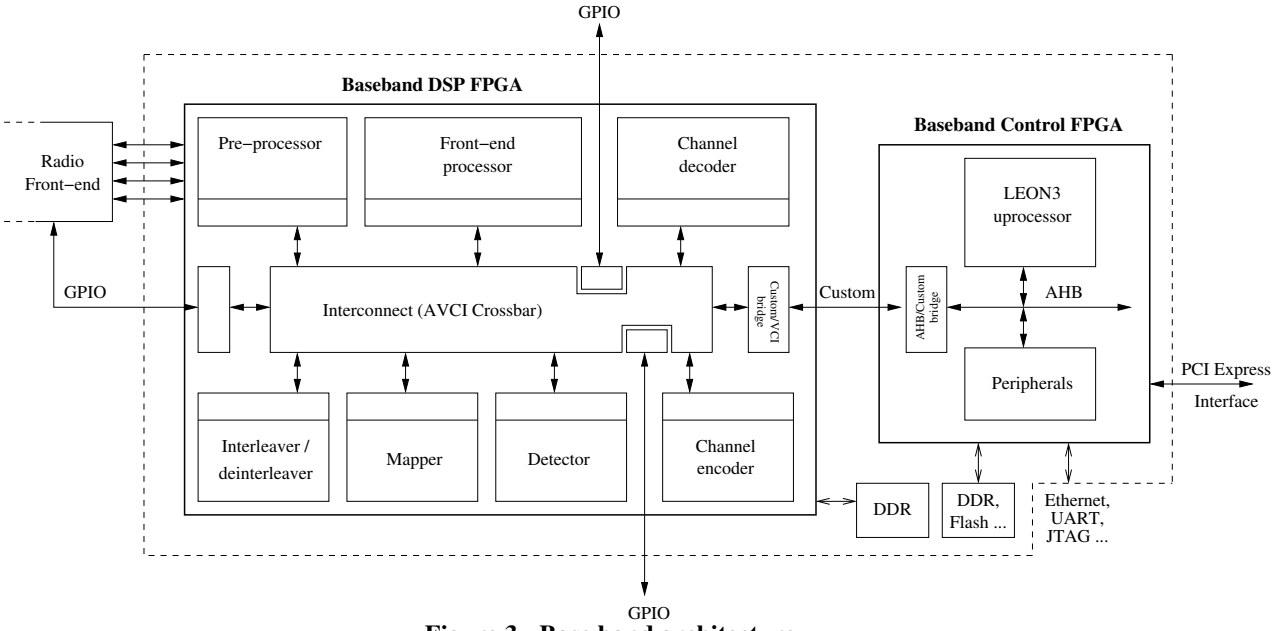

Figure 3 - Base band architecture

The 7 processing blocks of the DSP part are based on the same generic architecture, as depicted on Figure 4. The memory subsystem is a local memory space where input and output samples and parameters are stored. It is mapped on the global memory space of the system. The DMA engine has an initiator VCI interface and is capable of moving data blocks between any two memory locations in the system, local or not. Its configuration registers are also mapped on the global memory space. The VCI interface is the main control unit of the block. It is a target VCI component and embeds the control and status registers. Through this interface the micro-controller has full access to the local memory and internal registers. The IP core is the processing unit. It receives start orders and parameters from the VCI interface block and it directly accesses the memory subsystem through custom dedicated interfaces. The last component is an 8 bits micro-controller. It is enabled / disabled by the main micro-controller. Its memory space is the whole memory subsystem. It can be used to run sequences of processing and data transfers without any help from the main micro-controller, thus reducing the interrupt rate and workload. The IP core and the memory subsystem are specific to each block while the 3 other components are generic. The only custom interface is the set of communication channels between the memory subsystem and the IP core.

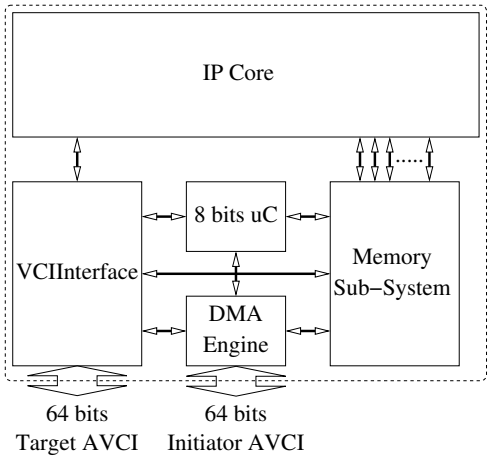

Figure 4 - Generic processing block architecture

The different processing units are:

- A pre-processor, interface with the AD/DA converters. It embeds a quadrature offset compensation unit, a digitally controlled oscillator, a retiming filter and programmable input - output FIFOs for fine grain synchronization.
- A Front-end processor. It implements DFT/IFT (from 8 to 4096 points, with a minimum throughput of one sample per cycle at 200 MHz), component wise additions, substractions, multiplications and divisions (between vectors or vectors and scalars), energy, max and argmax extraction and can also generate and process independently vector subbands.
- A generic mapper and detector for modulations BPSK to QAM256.
- A generic channel coder implementing any convolutional, or cyclic codes, plus M-sequences generation.
- A generic channel decoder (64 and 256 states Viterbi, UMTS and LTE turbo decoders).
- A generic interleaver – de-interleaver, up to 8 bits per sample, up to 8192 samples per permutation with rate matching, repeating and puncturing capabilities.

4. EXPRESSMIMO DIGITAL MOTHER BOARD

ExpressMIMO is the current hardware development platform for baseband Digital Signal Processing. It targets baseband signal processing for system complexities up to and including UMTS-LTE with up to 4 antennas. The card is still in the design process where it is being routed. We expect to have the first prototypes by early Fall 2008. This board includes several interfaces to a host PC and to the MAGALI daughter board as shown in TABLE 1.

FPGA Components	Virtex 5 LX330, Virtex 5 LX110T
Data Converters	4x AD9832 (dual 14-bit 128 Msps D/A, dual 12-bit 64 Msps A/D)
Precision Clocking	AD9510
MIMO Capability	4x4 Quadrature, 8x8 low-IF
Memory	128Mbytes/133MHz DDR (LX110T), 1-2 Gbytes DDR2 (LX330)
Configuration	512 Mbytes Compact Flash (SystemACE), JTAG
Bus Interface	PCIExpress 8-way

TABLE 1 – Main features of the ExpressMIMO Digital Mother board

5. MAGALI SOC

MAGALI chip of **Figure 5** is the successor of the FAUST chip of the beginning of the project. Based on a Network-on-Chip (NoC) architecture, it includes heterogeneous hardware blocs with specialized or generic functions.

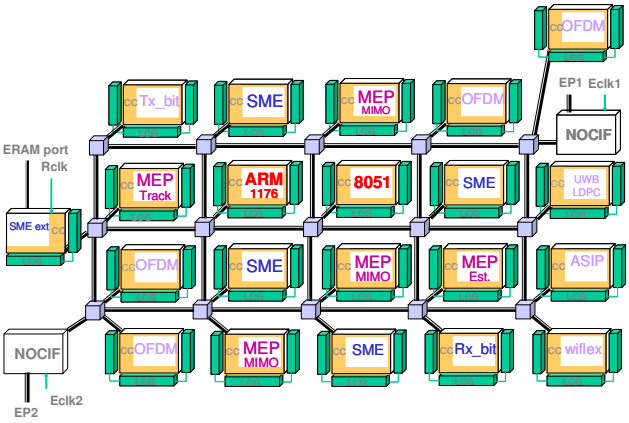

Figure 5 - MAGALI General view

MAGALI is implemented in a 65nm technology from STMicroelectronics. The NoC architecture gives the structure the required flexibility for SDR: operation scheduling, communication bandwidth dynamic allocation and on-line reconfiguration support are the main features allowed by the NoC framework.

The operation scheduling is performed locally, in each Communication and Configuration (CC) controller connected between an IP and the NoC. It consists of separated micro-programmable input, output flows and core running steps. It permits solving the synchronization issue locally, achieving high performances parallel processing.

The communication bandwidth dynamic allocation is a feature given by the Quality of Service (QoS) mechanism designed in the CC. Two channels of communication co-exist, allowing priority on the NoC and minimizing the communication latencies. A total aggregated bandwidth of 88 GO/s is available.

The on-line reconfiguration is a mechanism which allows, for an IP, to load its configuration from the outside in case of configuration miss. It permits a reduction of the needed memory inside each IP, as well as a fast reconfiguration to minimize application latencies.

Heterogeneous blocs are key solution to reach the goal of power/performance efficiency. As an example, powerful OFDM cores perform configurable framing/deframing with an IFFT/FFT computation in 15 µs for a 2K points FFT and 66 mW of consumption. Fast and flexible cores are used for channel coding algorithms, both for turbo-decoding and LDPC (blocks developed by University of Kaiserslautern, Germany). Dedicated DSP, called MEPHISTO are used for efficient matrix computation on complex numbers. They can

achieve 2.4 GMAC/s with less than 70 mW of power consumption. Thanks to embedded cordic and divider operators, they can perform complex algorithms for MIMO decoding, channel estimation and CFO tracking. Memory management units, called SME, are provided for data flow transformations, intermediate memorizing and IP configuration storing. Finally, an ARM core running an eCOS operating system is used for Medium Access Control (MAC) management.

As a conclusion, MAGALI is a powerful SDR baseband optimized for a large set of operating conditions in terms of power/performance ratio. The reconfiguration features of the NoC and the IP allow multi-application support as well as complex and diverse MIMO and OFDM schemes.

6. PARTIAL RECONFIGURATION OF FPGA

Partial reconfiguration of FPGA is a new feature that extends SDR perspectives while bringing the highest degree of flexibility to the HW domain. This permits to combine flexibility and processing power. This is allowed on the one hand thanks to very short time of reconfiguration. We have proven that it can go down to a few tens of microseconds to change an IP such as expected in a SDR context [4]. On the other hand, the necessity of an adequate management architecture is also required [5]. But this is not in the scope of this paper.

PR has been implemented in the context of the previous version of CEA NoC available at the beginning of the project: FAUST. However, all that has been defined and developed with FAUST is compatible with MAGALI, apart from a few implementation details. Figure 6 shows a structural view of the NoC extension and the FPGA sub-parts. PR is managed through 4 main elements:

- ICAP,
- Microblaze,
- SRAM to store the partial bitstreams,
- the PR IP themselves, encoder and mapper in this design example.

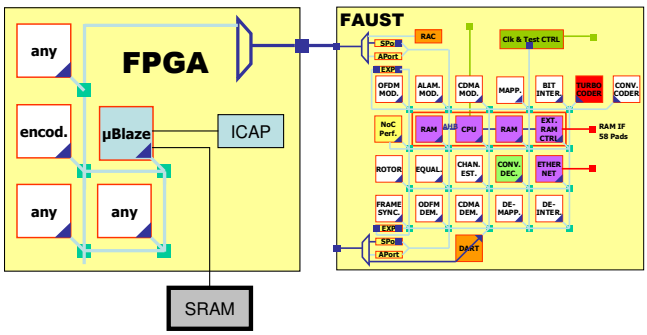

Figure 6 - FAUST NoC extension inside the FPGA for PR

As an example, the encoding processing merging encoder, interleaver and puncturer, has been shifted from the FAUST chip to the FPGA in order to become dynamically reconfigurable thanks to partial reconfiguration of FPGA. Experimentations show that there is no consequence on a real-time application QoS (a video stream for instance) whatever the chosen reconfiguration mode:

- FAUST encoding IP parameter change,
- FPGA encoding IP partial reconfiguration.

Reconfiguration time with PR approach has been measured and is of 700 µs.

7. ULTRA WIDE RF

From a RF point of view, the main objective of the proposed prototype is to show that a highly reconfigurable RF transceiver is possible with existing available components. Hence, the targeted prototype is very ambitious in term of frequency bands, since the objective is to address from 200 MHz to 7.5 GHz, with a maximum bandwidth of 20 MHz. Hence, we will be able to receive and transmit almost all the existing commercial Radio Access Technologies. Concerning the transmitted power, the target is comparable to existing GSM terminals (+21 dBm). On the receiver side, the objective is to have a noise figure from 8 to 12 dB, depending on the frequency band. The RF equipment includes up to 4 antennas and 4 RF chains. Finally, three keys features of the targeted prototype are:

- It will integrate advanced re-sampling functionalities.
- It will allow to communicate at the same time in different bands and different waveforms (A large scale of standards could be supported in terms of both processing power and RF capabilities: IEEE 802.11a-b-g-n, UMTS FDD, UMTS TDD, UMTS LTE, MC-CDMA, GSM, DVB-T, DVB-S, GPS, etc.).

8. COGNITIVE RADIO FUTURISTIC DEMO SCENARIOS

IDROMel project investigated very futuristic cognitive radio scenarios [6]. Two algorithms are proposed to illustrate the reconfiguration capacity of the IDROMel platform for cognitive radio and will be included in the scenario. These algorithms are the detection of vacant frequency bands [7] (Spectrum Sensing) and MUD-MLSE receiver for overlapping interference [8] (Interference Rejection).

8.1. Detection of vacant frequency bands

One of the practical interests of SDR equipment is its ability to switch between different radios technologies by searching vacancy band. For this, the algorithm of detection of vacant frequency band has been developed. This opportunistic access to spectrum permits to find vacant channels within

which the terminal can transmit and receive. The process is resumed by the test for presence of any telecommunication signal within a given frequency band. Any telecommunication signal can be detected by testing the presence of the cyclostationary property. It is based on a chi-squared statistical test. However, in a cognitive radio context, the algorithm must improve its ability to detect weak signals to prevent the band spectrum exploitation already used by a primary user.

8.2. MUD-MLSE receiver for overlapping interference

Most of standards suffer now a lack of radio resources. These constraints imply a lack of spectral resources given the target QoS and roll-off density to reach. In this context, two cases of interference can clearly be distinguished: strong co-channel interference (CCI) and partial channel interference (PCI). First, an aggressive roll-out pattern with strong co-channel interference is being deployed. Second, a less stringent roll-out pattern is being pertained, and then interfering frequency bands partially overlap with the band of interest. The system model with an appropriate MLSE is used, where we have augmented the branch metrics to facilitate causal implementation. We will deal with binary phase shift keying (BPSK) modulation schemes only. For the interference rejection, the proposed MUD-MLSE detector in the context of heterogeneous WLAN-like channels allows to obtain good performance in the overlap configuration. The next step of the work will be improve and large the functionality for each part of the demonstration.

9. CONCLUSION

In this paper, an overview of the IDROMel project is presented. The main objective of the project is to build an SDR platform for new wireless communication standards. In addition, our final goal is to show that a flexible basestation or mobile terminal will become technically feasible in a couple of years. Of course, there is still a considerable effort required in terms of power consumption, size, etc. Hence, many technical problems still need to be solved. Moreover, and this is probably the most difficult issue, some other problems are to be solved, such as regulation, security, etc., in order to allow the SDR equipment to become a reality in everyday life.

10. ACKNOWLEDGMENT

Authors want to thank the French ANR program for its support to the IDROMel project.
This work was also supported by the European Commission in the framework of the FP7 Network of Excellence in Wireless COMmunications NEWCOM++ (contract n. 216715)

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