TEXAS TECH UNIVERSITY™

Sample Clock Offset Detection and Correction in the LTE Downlink Receiver

Elliot Briggs[1], Chunmei Kang[2],
Amit Mane[2], Dan McLane[2], Brian Nutter[1]

SDR'11 - WinnComm Europe
Brussels, Belgium June 22nd – 24th

Innovative Integration
a subsidiary of ISI
... real time solutions!

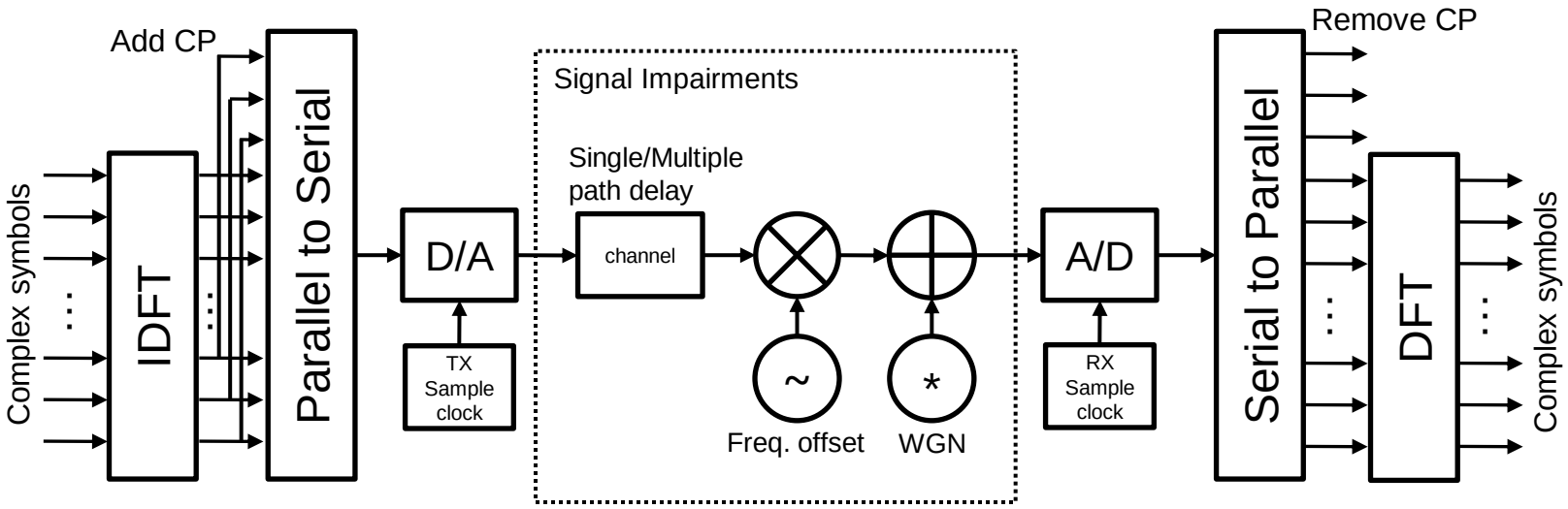
1: Texas Tech University, 2: Innovative Integration

Presentation Overview

- OFDM Receiver Synchronization Basics
- Mechanics of Sample Clock Offset
- Sample Clock Offset Detection
- Developed Sample Clock Correction Technique
- Results

OFDM Receiver Synchronization Basics

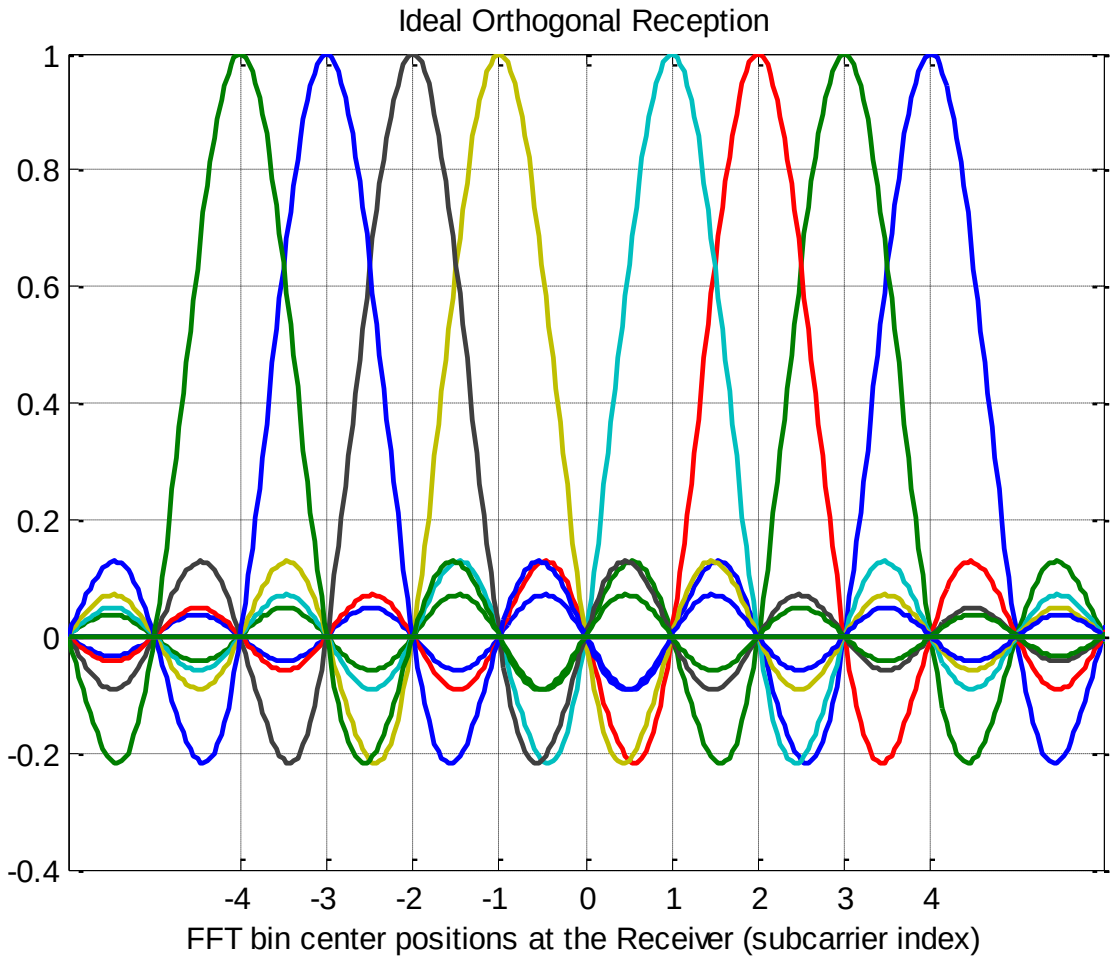
Traditional OFDM model example:



Impairments:

- AWGN: weak (noisy) signal
- Frequency shift: errors in RF electronics (TX and RX)
- Delay: Asynchronous startup time, multiple paths
- Sample Clock Offset?

OFDM Receiver Synchronization Basics

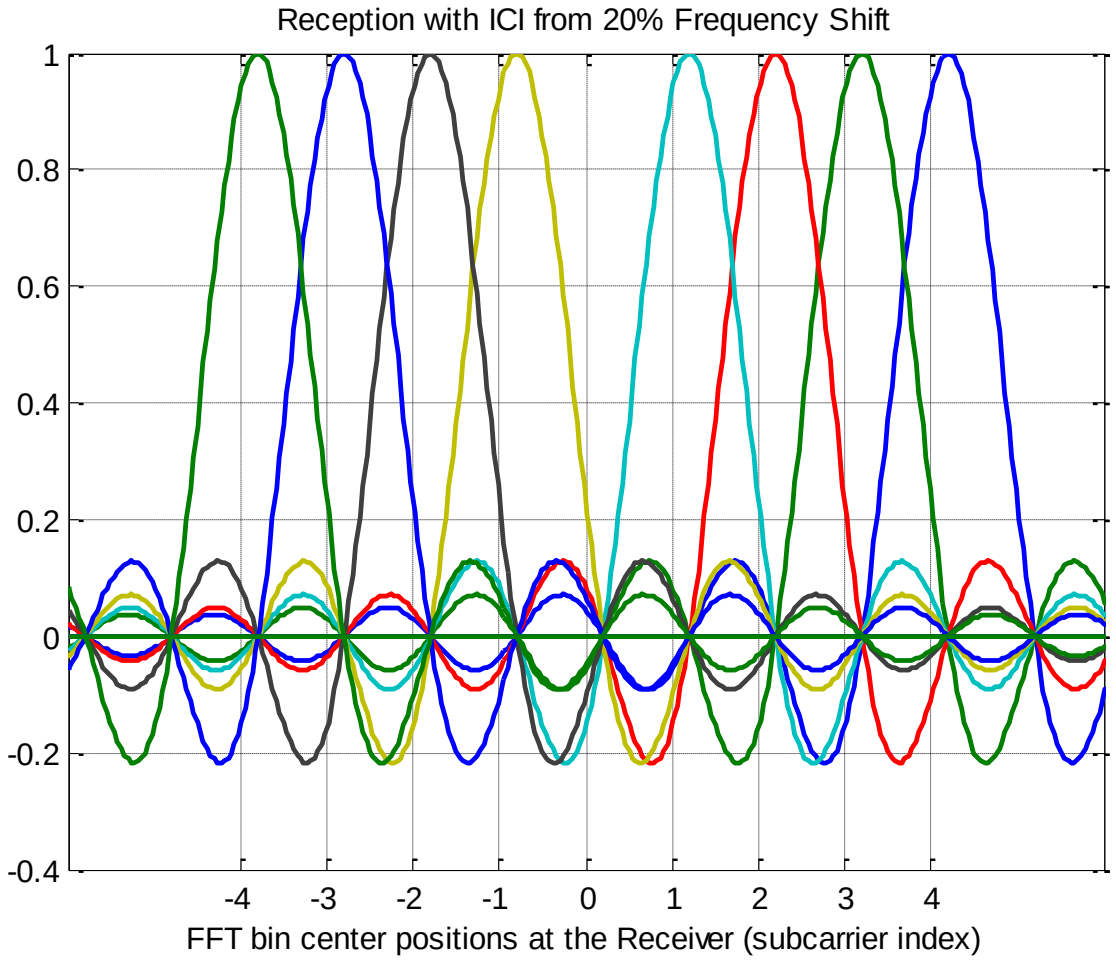


Ideal OFDM Reception:

•The receiver's FFT bins are aligned with each subcarrier

• Here, at the receiver, each subcarrier is orthogonal to the others

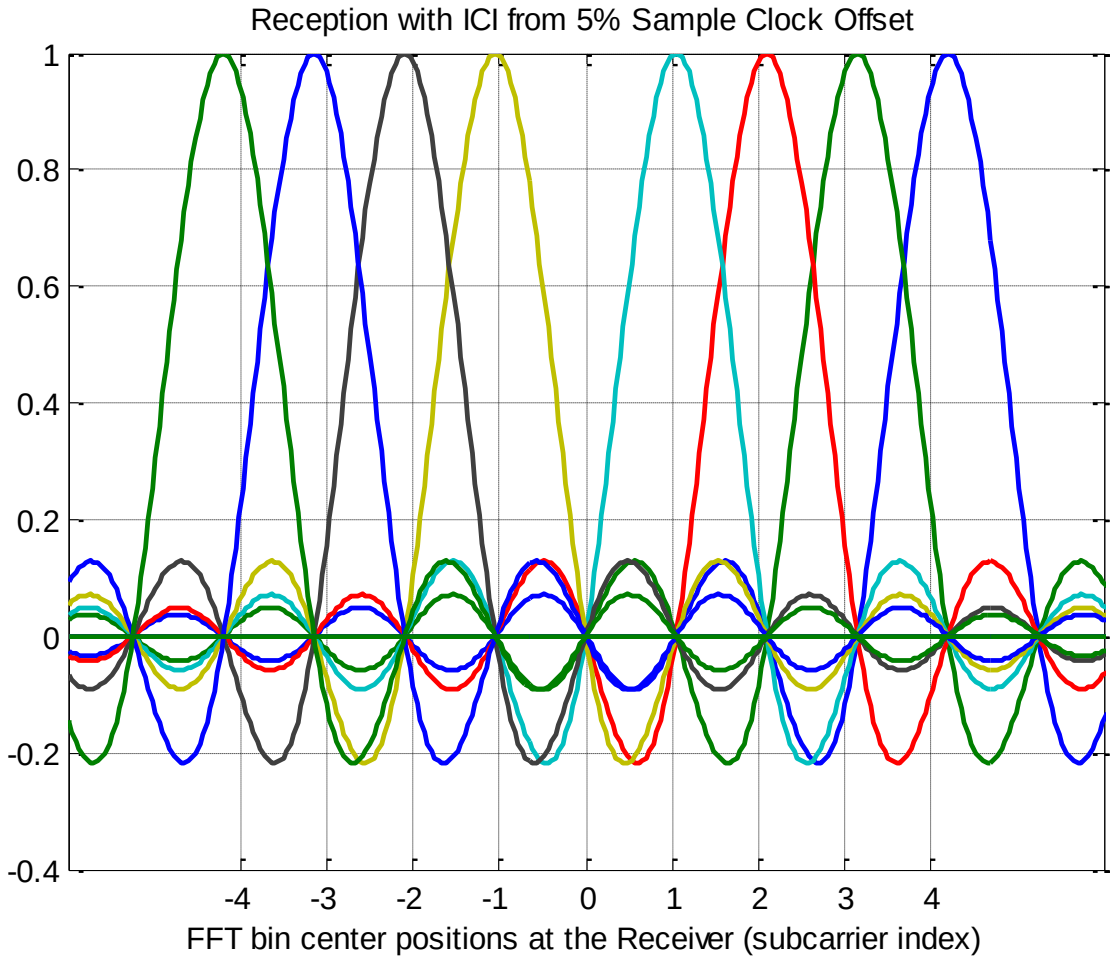
OFDM Receiver Synchronization Basics



OFDM Reception Affected by Frequency shift:

- Each FFT bin is misaligned by an equal amount
- Each received subcarrier experiences the same amount of ICI

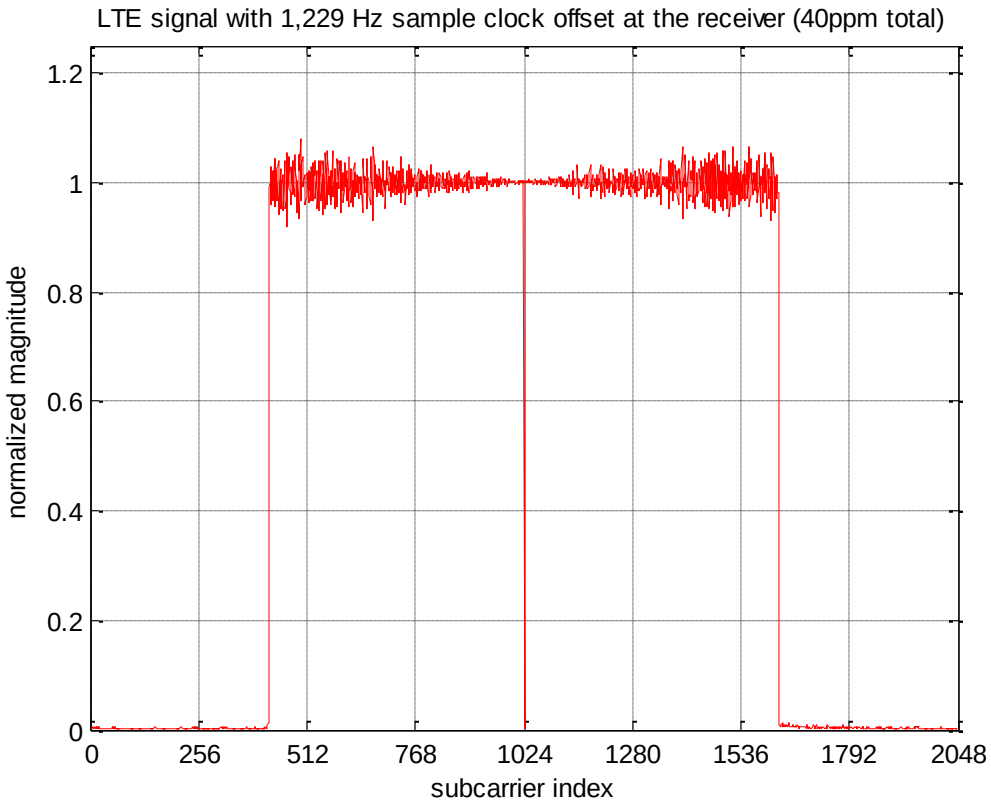
OFDM Receiver Synchronization Basics



OFDM Reception Affected by Sample Clock Offset:

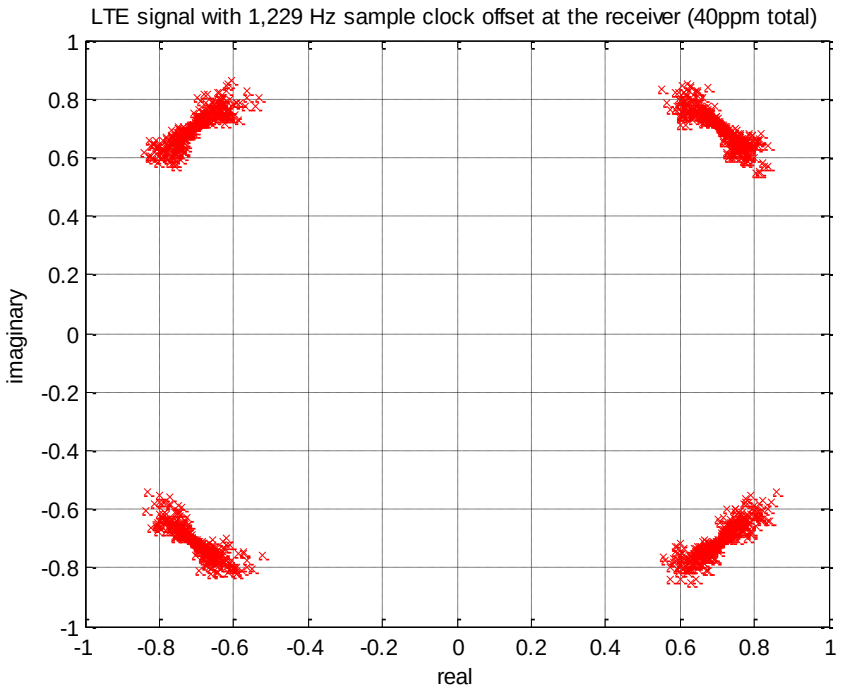
- Each FFT bin has a cumulative amount of shift
- The outer subcarrier positions experience the most ICI

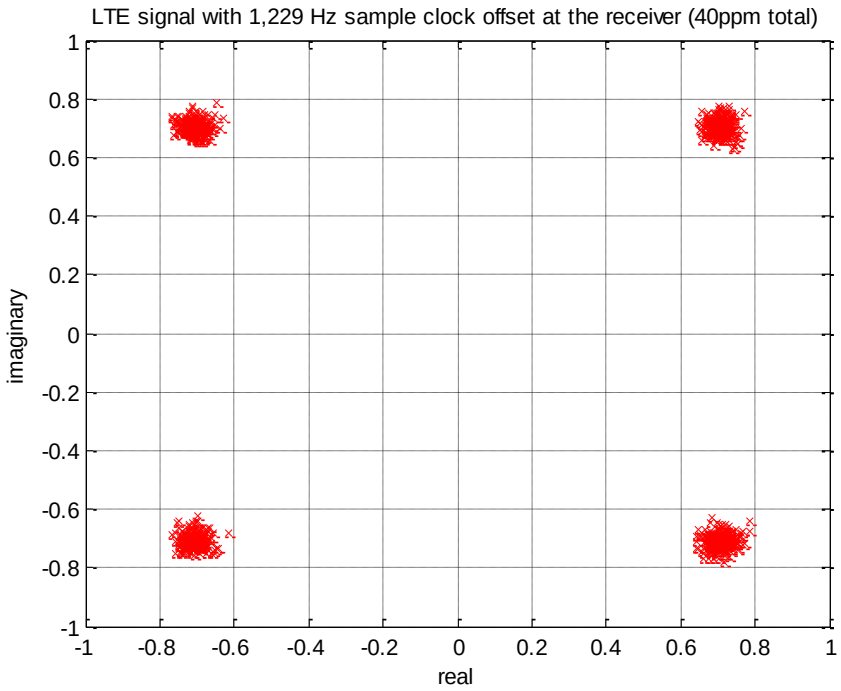
OFDM Receiver Synchronization Basics



- 40 ppm error at the receiver simulates the maximum error from 20 ppm clock oscillators at the transmitter and receiver
- 40ppm = 1.229 kHz , 8.2% of one subcarrier spacing
- Here, the SNR is 50 dB before the sampling clock error is added

OFDM Receiver Synchronization Basics

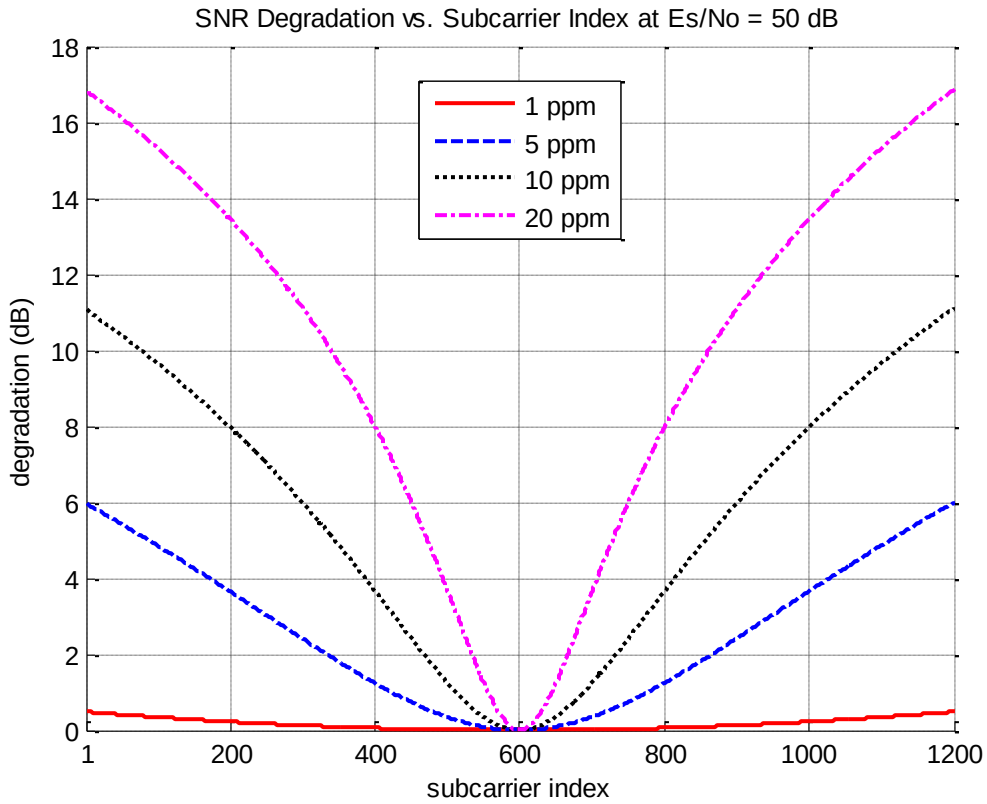




- A slight phase shift occurs from fractional timing offset
- The outer subcarrier positions are no longer orthogonal and contain energy from neighboring subcarriers

- After the phase is unwound, only the ICI component remains
- The ICI appears as noise at the outer subcarrier locations

OFDM Receiver Synchronization Basics

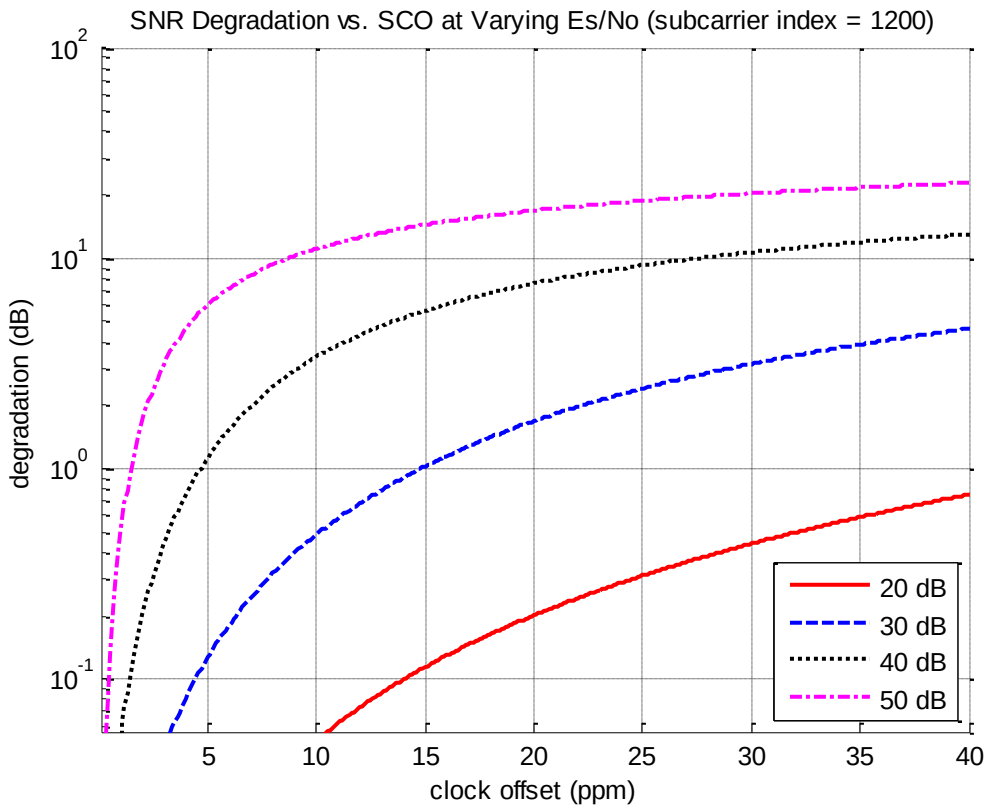


- ICI causes SNR degradation which is the most severe at the outer subcarrier locations.

- Even a 5ppm sample clock error can cause 6 dB of degradation when Es/No = 50 dB

$$D_n \approx 10\log_{10}\left(1+\frac{1}{3}\frac{E_s}{N_o}\left(\pi 10^{-6}\Delta f_s\right)^2\right) \quad [1]$$

OFDM Receiver Synchronization Basics

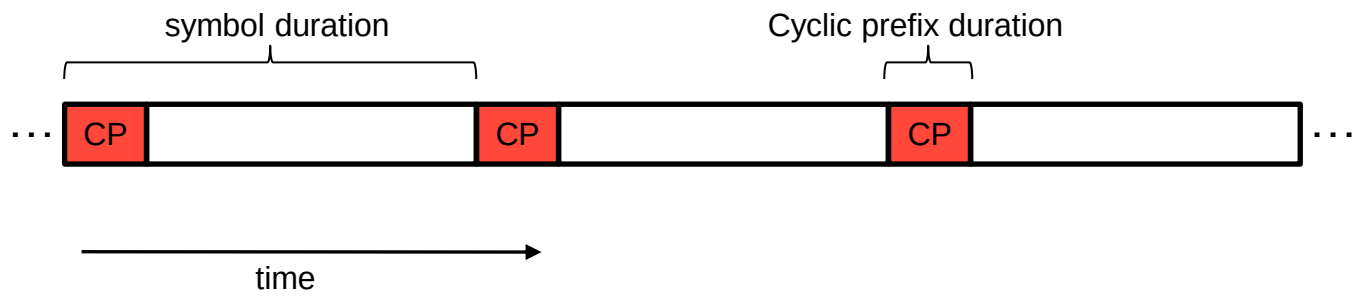


- The level of degradation is displayed for several levels of SNR

- The SNR is adversely affected, even with modest clock offsets

Mechanics of Sample Clock Offset

Transmitted OFDM symbols:



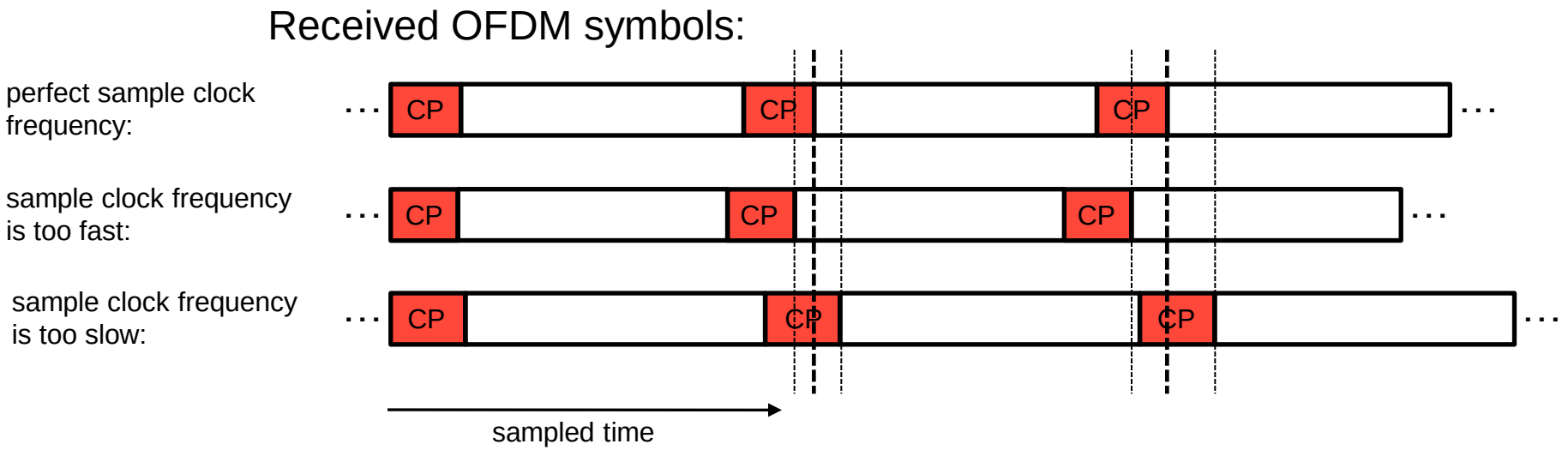
LTE Example:

- "Extended" cyclic prefix mode
- 20 MHz mode
- Ideally, each symbol lasts only 83.33 μs

$$T_s = 1/30.72\,\text{MHz}$$
$$N_{CP} = 512$$
$$N_{FFT} = 2048$$
$$T_{symbol} = (N_{CP} + N_{FFT})\,T_s = 83.33\mu\text{s}$$

[2]

Mechanics of Sample Clock Offset



- 2560 samples will take a longer or shorter amount of time for the receiver to collect, depending on the offset conditions

$$T_s = 1/30.72\text{MHz} + 1/f_{error}$$

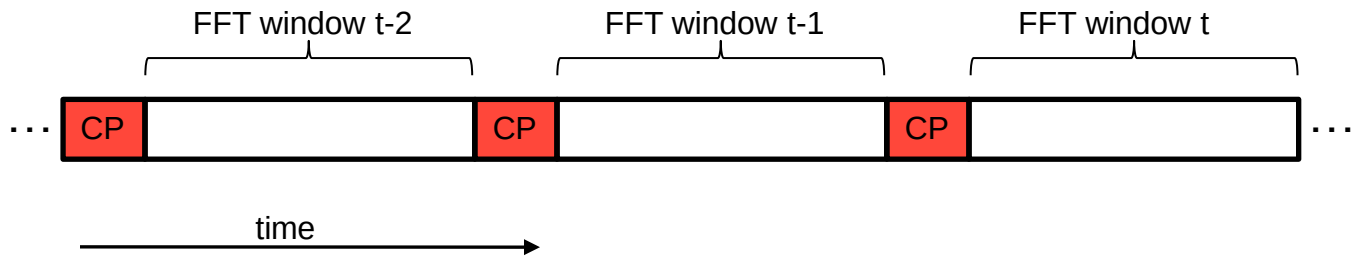
$$T_{symbol} = (N_{CP} + N_{FFT})T_s \neq 83.33\mu\text{s}$$

- The rate that the symbols drift from the perfect case directly indicates the sampling clock offset magnitude.

- The direction in which the symbols drift indicate the sampling clock offset direction

Sample Clock Offset Detection

Any DFT-based OFDM system must have an FFT window timing synchronization component to properly align the FFT window



Any FFT timing synchronization method can give sample clock offset information

- Using the LTE Primary Synchronization Signal (PSS)
  - Timing information provided every 5 ms
- Cyclic Prefix Correlation
  - Timing information provided every 83.33 μs

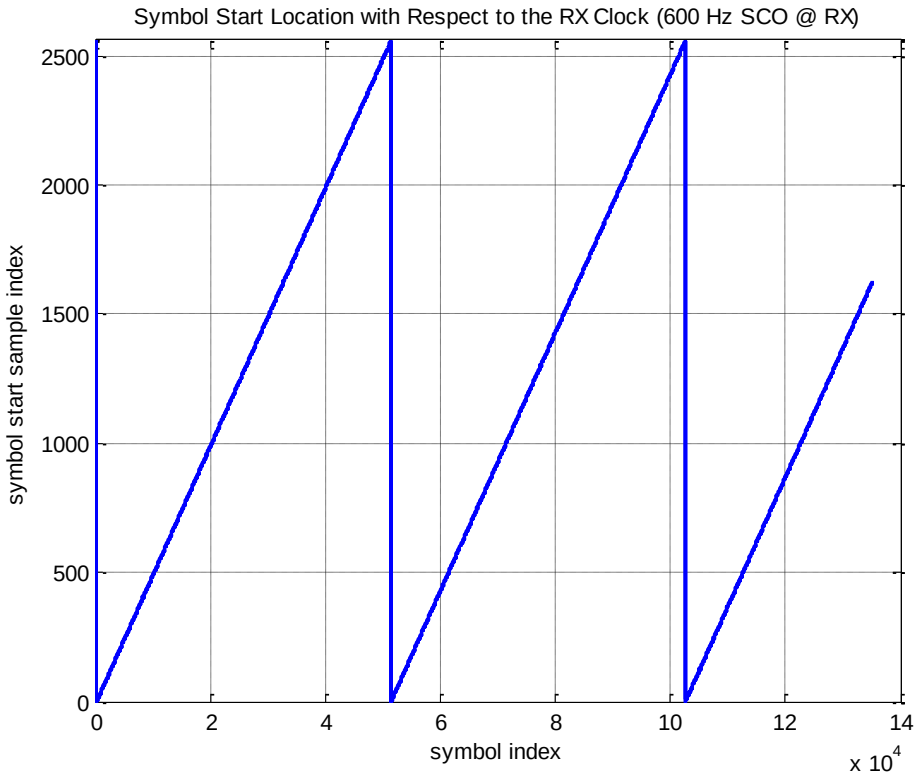
Sample Clock Offset Detection

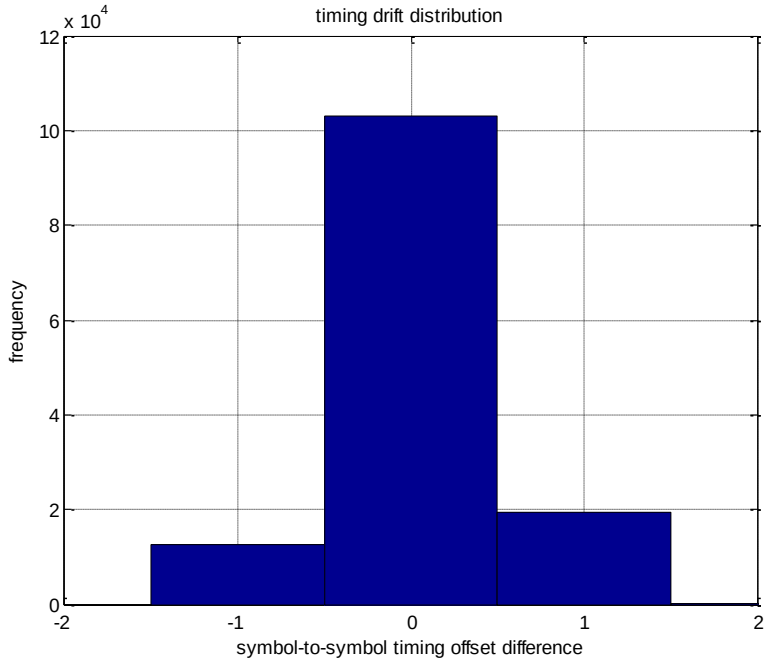
Example: (-)+100 Hz clock offset error:

- Generates (removes) 100 extra samples per second.
- This will generate (remove) 1 sample for after 120 OFDM symbols, or 0.0083 samples to each symbol
- A +12 kHz clock offset will generate an entire sample for each OFDM symbol

$$f_{error}[n] = \frac{12{,}000}{N} \sum_{t=1}^{N} \left(S_{offset}[n-t] - S_{offset}[n-t-1] \right)$$

Sample Clock Offset Detection



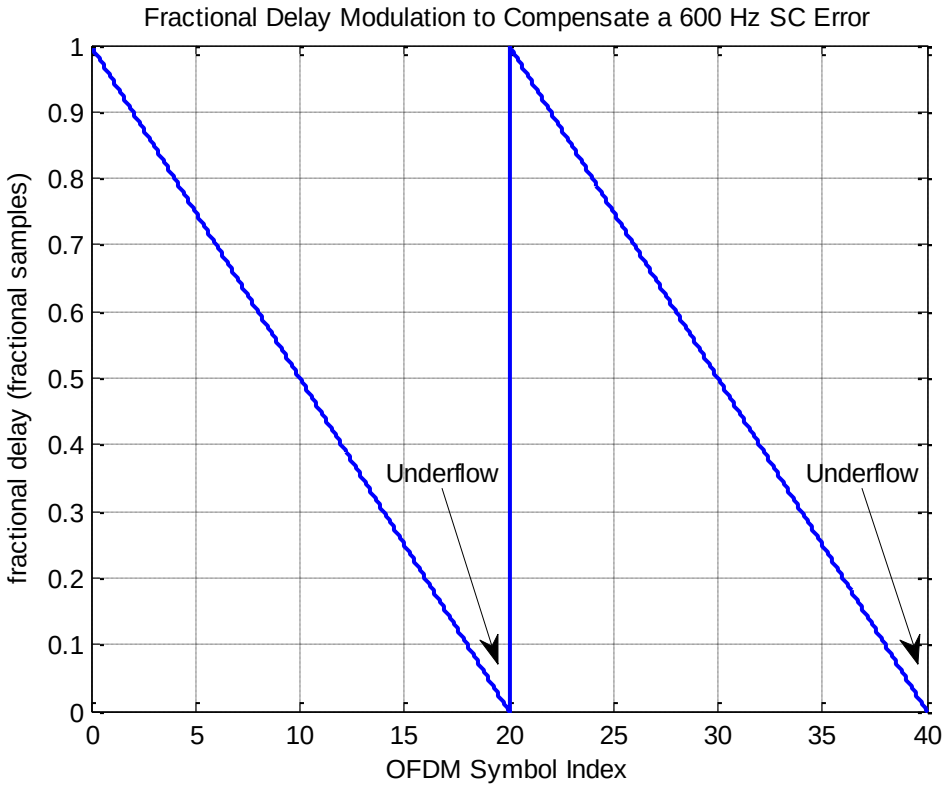


$\mu = .05$

$$n = N = 135{,}000$$

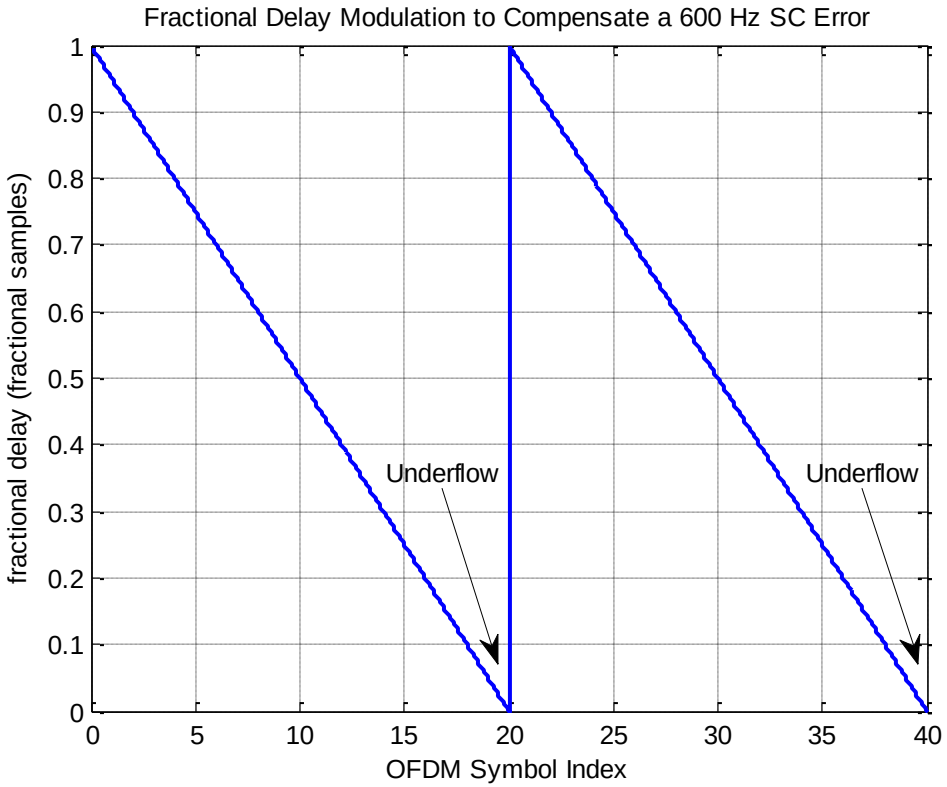
$$f_{error}[n] = \frac{12{,}000}{N} \sum_{t=1}^{N} \left(S_{offset}[n-t] - S_{offset}[n-t-1] \right) = 12{,}000 \times .05 = 600 \text{ Hz}$$

Sample Clock Offset Detection



- SCO can be corrected if the signal is resampled at the correct sampling rate
- Modulate the fractional delay value at every sample to effectively resample the signal
- When the fractional delay value over/underflows, repeat/skip a sample

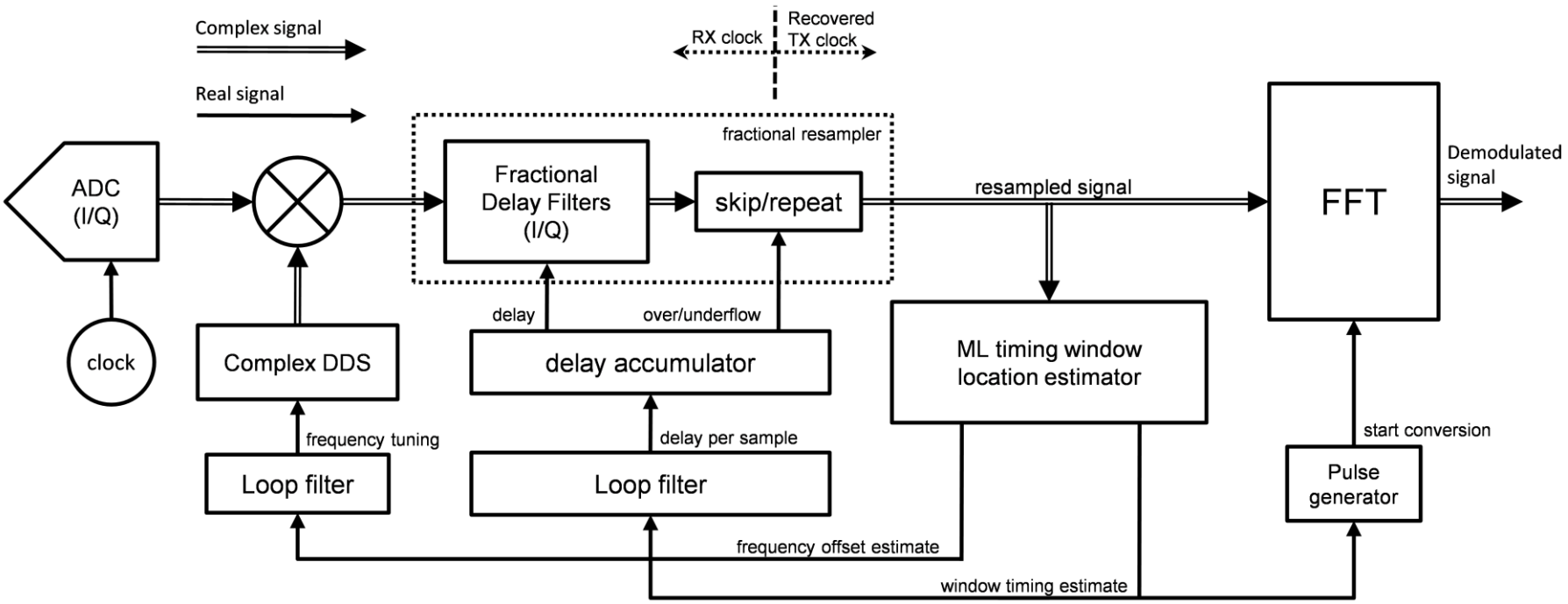
Developed Sample Clock Correction Technique



The resampler “compresses” the signal by continuously reducing the delay for each sample

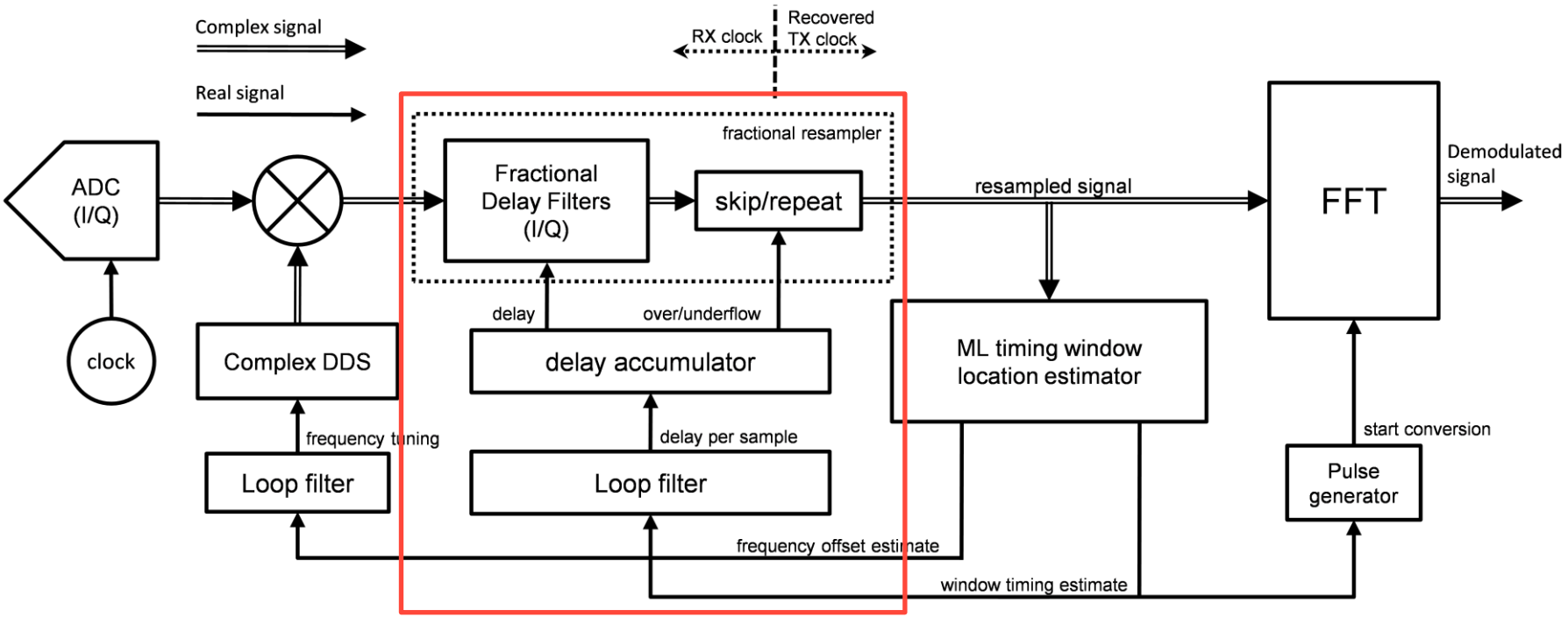
- In this example, each sample has a -.05/2560 delay difference from the previous sample to correct the .05/2560 from the sample clock offset.
- When a negative delay is requested, a sample is skipped.
- Here, fewer samples are produced at the output of the resampling filter than are input
- Ideally, the resampler produces 2560 samples per 83.33 μs
- The signal should have stationary symbol timing after resampling

Developed Sample Clock Correction Technique



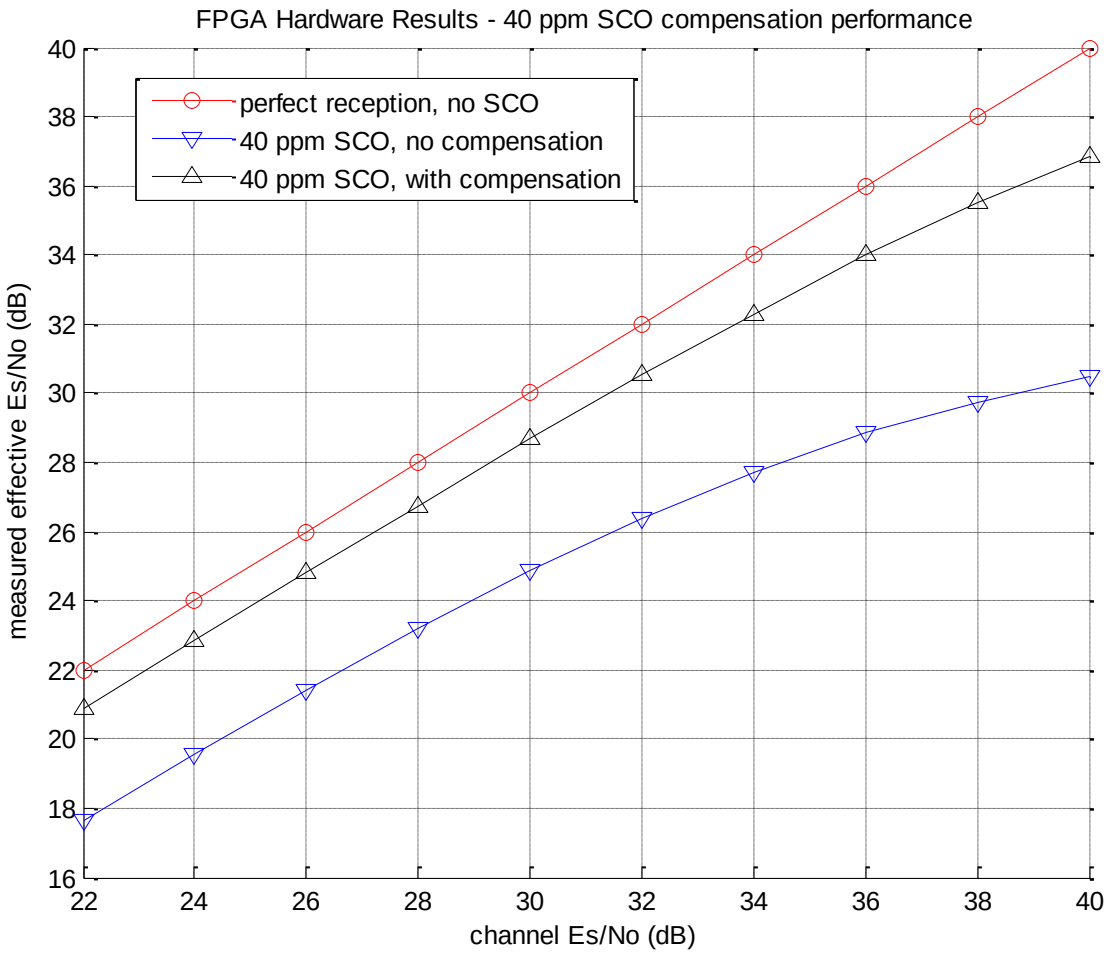
- The ML timing and frequency offset estimator [3] uses the cyclic prefix
  - The timing estimate is used by the loop filter and to trigger an FFT conversion
  - The frequency offset estimate is used to correct residual frequency shift

Developed Sample Clock Correction Technique



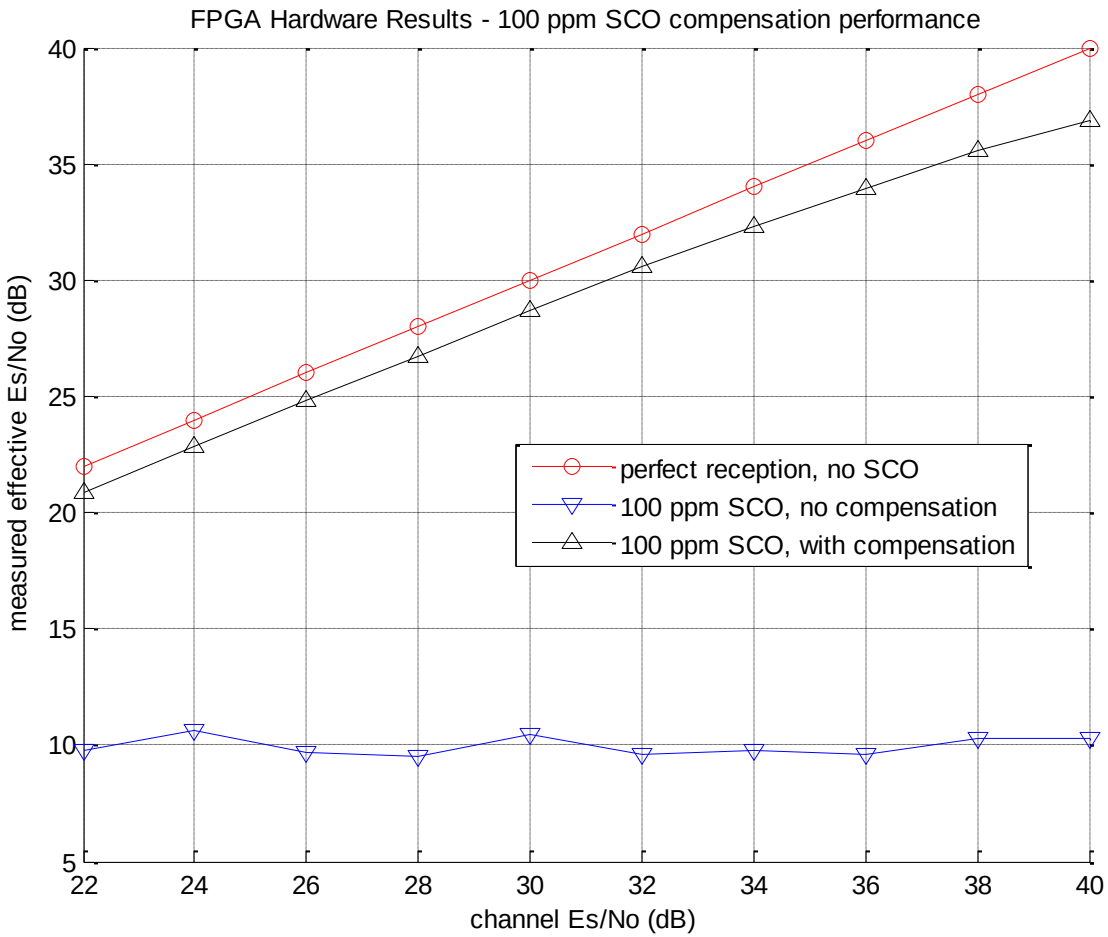
- The receiver uses feedback correction to adjust the symbol timing and frequency correction
- The timing loop filter averages many timing estimates to get an average window drift rate, just as in the previous example
- The delay accumulator constantly accumulates fractional delay and modulates a fractional resampling filter

FPGA Hardware Implementation Results



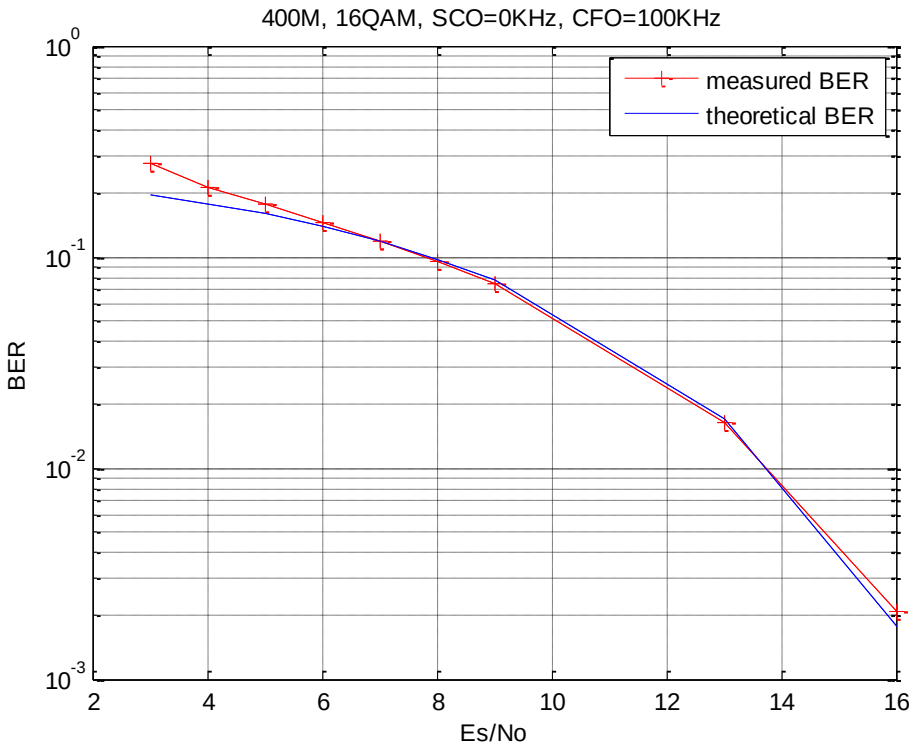
- Design implemented in an X5-400M FPGA board by Innovative Integration
- Two separate clocks are used, the frequency difference is measured
- With SCO compensation enabled, the minimum SNR gain is around 3 dB
- SNR gains increase at higher values of Es/No (~ 6 dB)!

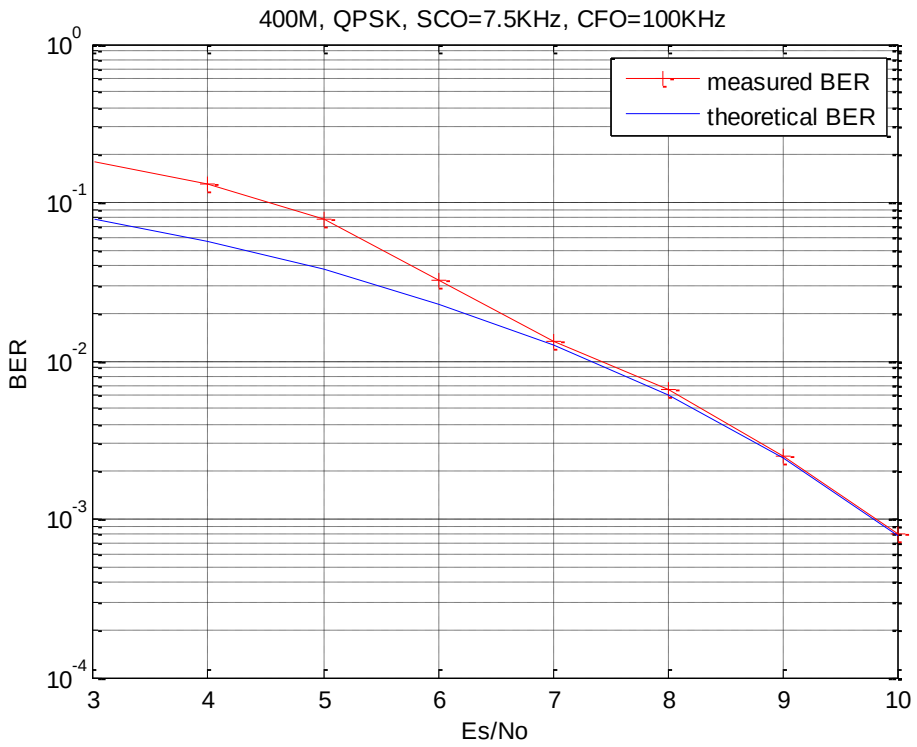
FPGA Hardware Implementation Results



- A hidden advantage to this correction technique exists
- CP correlation reliability is reduced when the sampling clock changes a significant amount in a single symbol duration
- Without SCO correction, the timing synchronization fails
- With SCO correction, the SNR values are almost identical to the 40 ppm case at 100 ppm
- The algorithm has been tested to track as much as a 7.5 kHz sample clock error (~250 ppm)!

FPGA Hardware Implementation Results





- CFO = 100 kHz : frequency shift of over 13 subcarrier spacings
- SCO = 7.5 kHz : ~250 ppm sampling clock offset

FPGA Hardware Implementation Results

Corner Cases:

- Maintains timing lock down to 3dB SNR

- Maintains receivability:
  - LTE cell ID decode, frame sync successful
    - SNR = 5dB
    - CFO = ±75 kHz (± 5 subcarrier spacings)
    - SCO = ±4 kHz (±133.33 ppm)

Conclusions

- The developed SCO measurement and correction method allows the LTE user equipment to be equipped with a lower cost, less precise sample clock source.
- Any timing synchronization algorithm can be employed to generate sample clock offset measurements to be used for correction
- The measurement and correction is in the *time domain,* so the algorithm is agnostic to any frequency domain information (reference symbols, training, etc).
- Can be applied to any OFDM-based standard

Conclusions

- May be useful for surveillance applications, maximizes OFDM signal reception quality for any OFDM signal

References

[1] T. Pollet, P. Spruyt, and M. Moeneclaey, "The BER performance of OFDM systems using non-synchronized sampling," *Proceedings of the IEEE Global Telecommunications Conference (GLOBECOM'94)*, San Francisco, USA, November 1994, pp. 253-257.

[2] 3GPP TS 36.211 V8.9.0 “Physical Channels and Modulation”. Rel. 8.

[3] J.J. van de Beek, M. Sandell, P.O. Börjesson, "ML Estimation of Time and Frequency Offset in OFDM Systems," *IEEE Transactions on Signal Processing*, Vol. 45, No. 7, July 1997, pp. 1800 - 1805.