Porting of an FPGA Based High Data Rate DVB-S2 Modulator

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SDR'11 WInnComm

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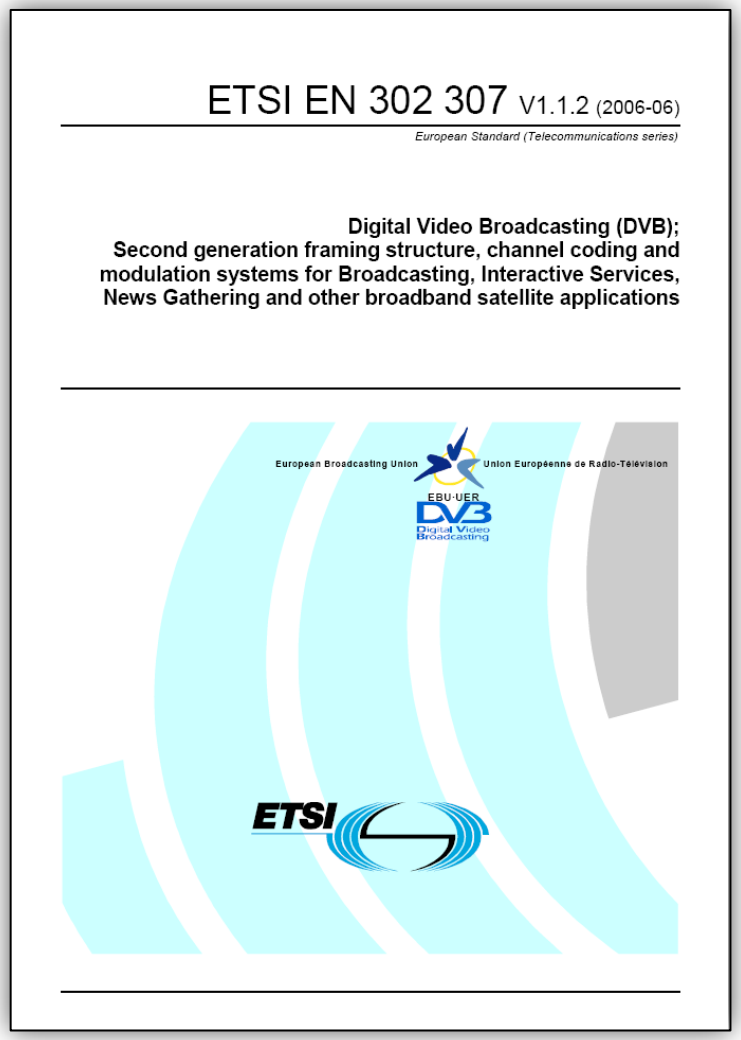
Outline

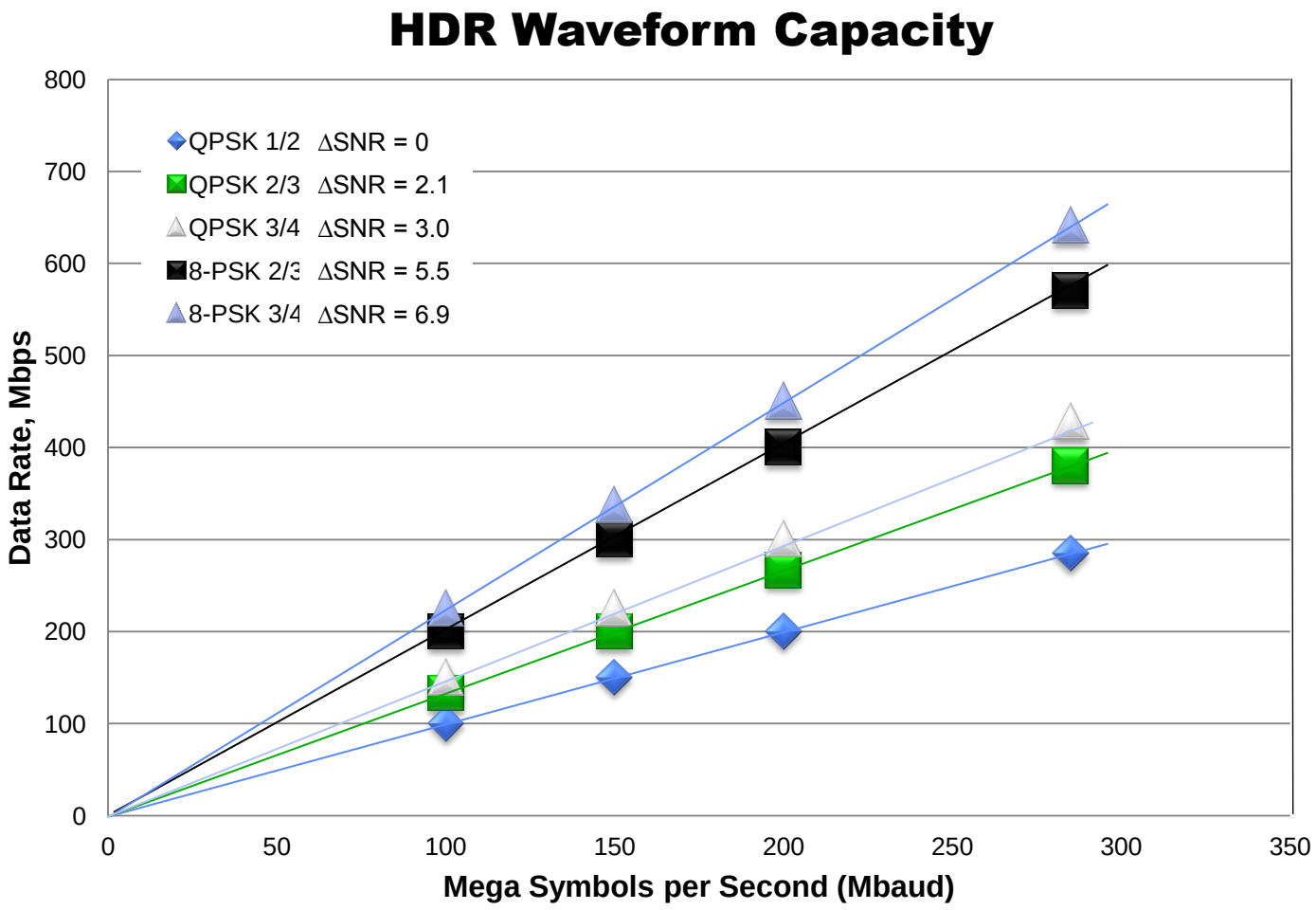
- **High Data Rate DVB-S2**
- **Waveform Description**
- **BDR-1 and the Porting Effort**
- **Over-the-Air Testing**
- **Conclusion**

The High Data Rate DVB-S2 Waveform



- **DVB-S2 is the second generation digital video broadcasting standard from the ETSI (European Standard Telecommunications Series)**
  - **Flexible input stream** adapter, suitable for operation with single and multiple input streams of various formats (packetized or continuous)
  - **Powerful FEC** system based on LDPC (Low-Density Parity Check) codes concatenated with BCH codes, operating 0.7 – 1 dB dB from the Shannon limit
  - **Wide range of code rates** (from 1/4 up to 9/10); allows "tunable" power- and spectral-efficiency
  - **Broad industry base** with successful commercially, available, implementations which support data rates up to ~50 Msymbols/s
- **HDR DVB-S2 Implementation supports a subset of the standard at much higher symbol rates**
  - QPSK, 8PSK
  - 1 to 280 Msymbols/s

HDR Waveform Modes and Rates



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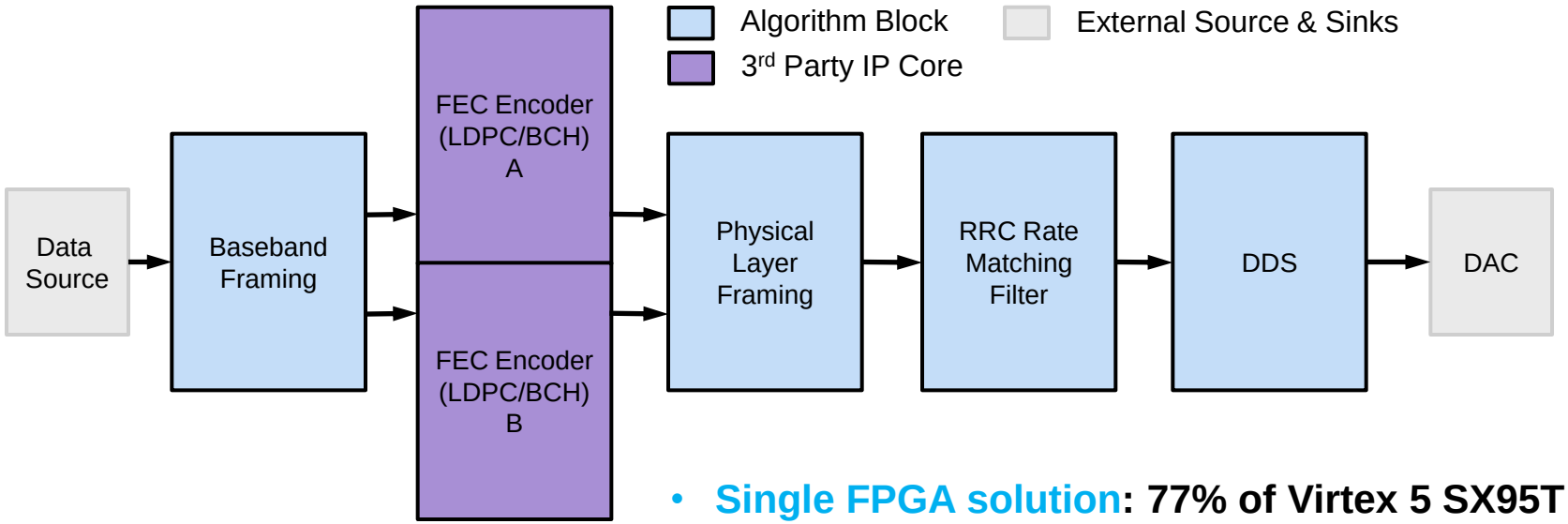
HDR Modulator Architecture

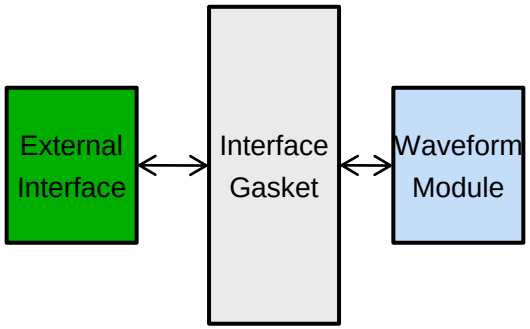


Extensive capabilities, leveraging modern technology to deliver a portable SWaP-compliant system

- **Single FPGA solution: 77% of Virtex 5 SX95T**
- **Consumes < 40 Watts at full rate**
  - **Includes: Gigabit Ethernet, FPGA, and high-speed DAC**
- **Dual SRRC real filters on I and Q channels**
  - **Supports rate matching from 1 to 280 Msps, in 2^{32}-1 steps**
- **Direct digital synthesis of L-band IF**
- **Architecture independent FEC Encoder pending**

External Interfacing

- To enable easier porting the waveform interfaces are generalized
  - System interface
    - Clocks, resets, etc.
  - Host interface
  - Data interface
    - Input data, DAC signals
- The original development platform design is provided as an example to the porting team
- Porting team is required to develop *Gaskets* to bridge between their hardware platform and the waveform module



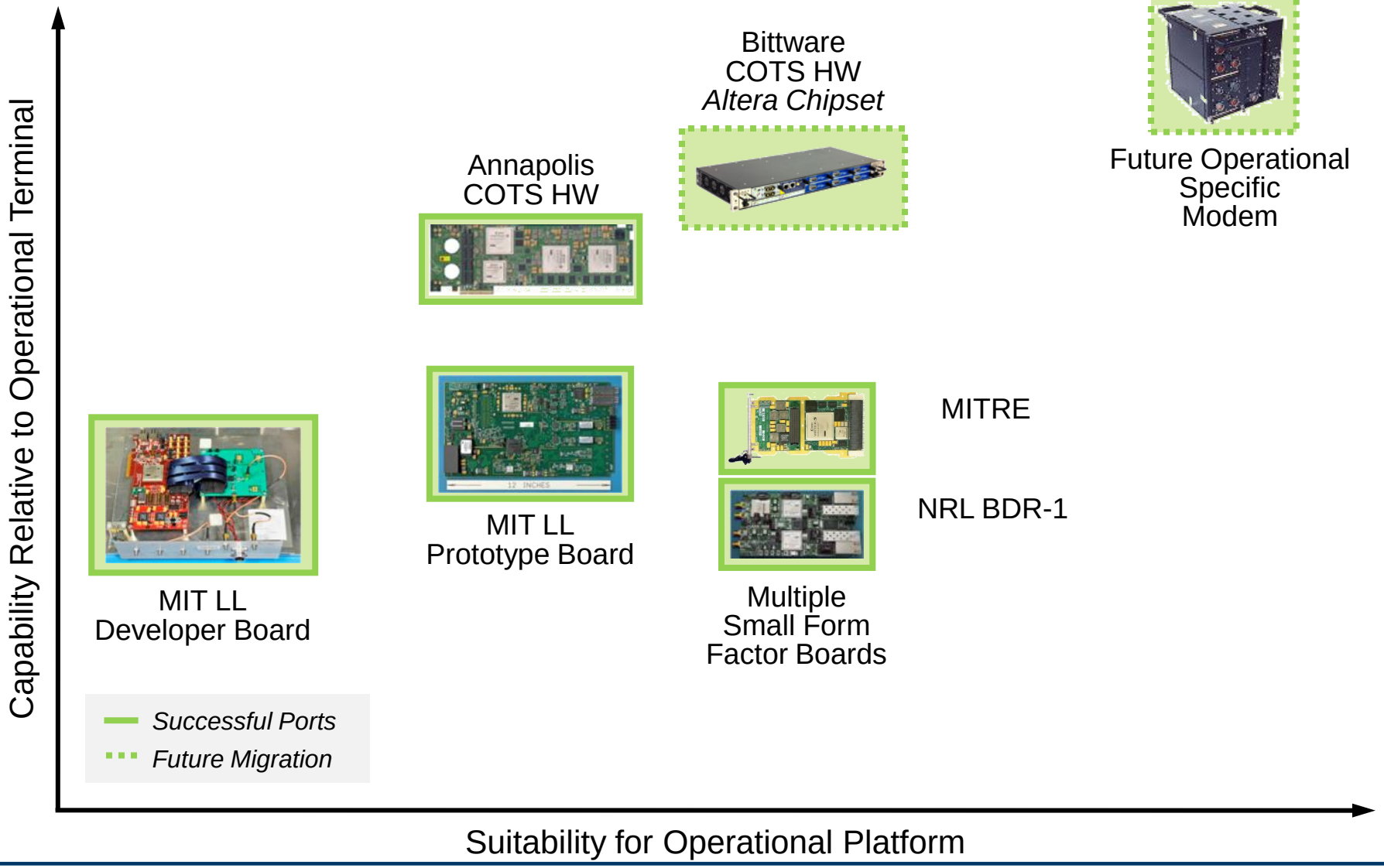
Modulator FPGA Sizing

- **The modulator components were successfully targeted to various FPGAs ranging from a Virtex 5 SX240T to a Virtex II Pro 100**
- **The Virtex 5 SX240T resource utilization is as follows:**

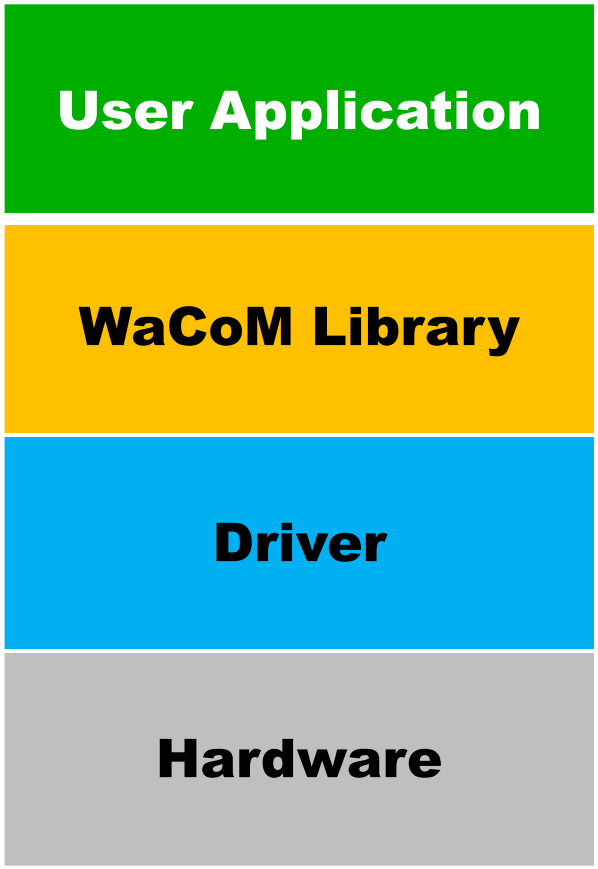
Module Name and Path	Registers	6-input LUTs	BRAM (32kb)	DSP48s
Tx Core, direct conversion DAC, Xilinx FEC /modules/tx_core	21k	20k	111	20
Tx Core, direct conversion DAC, AHA FEC /modules/tx_core	38k	39k	225	16
Tx Core, I/Q DAC, Xilinx FEC /modules/tx_core_no_cm	20k	19k	92	4
Tx Core, I/Q DAC, AHA FEC /modules/tx_core_no_cm	37k	38k	209	0

Multiple versions, using the same code base, to support a wide variety of possible platforms.

Waveform Implementations of the High Data Rate Modulator



WaCoM Software Stack



This illustrates how the WaCoM library is typically situated with respect to other software layers.

The user application (or GUI/CLI) relies on the WaCoM library which in turn relies on the user-supplied platform-specific driver implementation.

The "driver" either communicates directly with the hardware, or indirectly through additional software or operating system layers.

WaCoM is a layered approach which aims for maximum software reuse.

WaCoM Library

Abstracts and encapsulates the software/hardware interface

- C++ library that provides a modulator controller object
- Programmer does not require knowledge of modulator internals
- Below is a simplified example of setting the center frequency

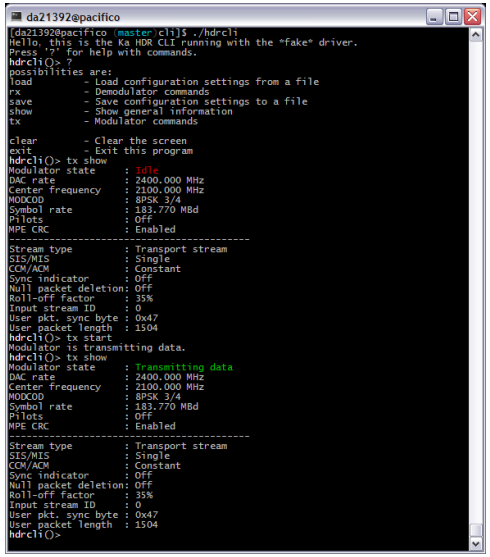
Instead of this:

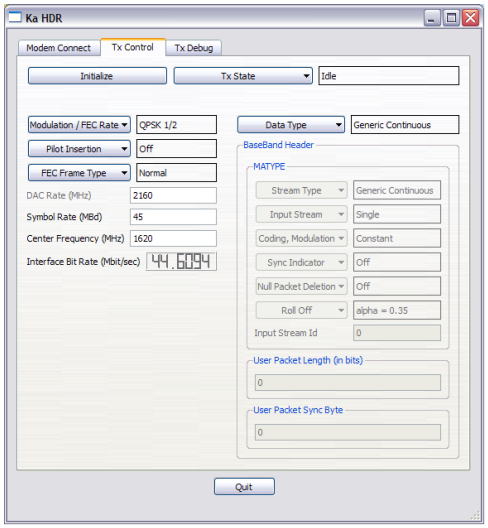
```
// Disable everything
prev = ReadReg32(ENABLES_REG);
WriteReg32(ENABLES_REG, 0x0);

// Write center frequency register
center = ReadReg32(CENTER_FREQ_REG);
center &= 0xffff0000;
center |= freq * multiplier;
WriteReg32(CENTER_FREQ_REG, center);

// Restore previous state
WriteReg32(ENABLES_REG, prev);
```

WaCoM library allows this:

```
// Set center frequency
controller.setCenterFrequency(freq);
```

User Interface





- **WaCoM library contains no UI code**
- **Reusable GUI and CLI exist**
  - **Designed to be used with WaCoM library**
  - **Usually require adaptation for platform-specifics**
    - **Loading FPGA images**
    - **Connecting to modem**
    - **e.g. over a network**
  - **Can be used as example code or as starting point**

Waveform Artifacts

Waveform Description

Description

Waveform Functional Specification
ESC-HDRAT-MIT-LL_Waveform-Functional-Spec_25Jan11_Rel1.pdf

Waveform Design Specification
Waveform-Design-Specification_25Jan11_Rel1.pdf

Waveform Development Environment
Waveform-Development Environment_25Jan11_Rel1.pdf

Models

C++ Model
Waveform_Model-C++_25Jan11_Rel1.zip

Mathworks Model
Waveform_Model-Mathworks_25Jan11_Rel1.zip

Modulator Model Overview
Modulator-Model-Overview_HY-JH_25Jan11_Rel1.pdf

Waveform Implementation

VHDL/HW

VHDL
Waveform_VHDL_25Jan11_Rel1.tar.gz

VHDL Modulator Firmware Description
VHDL-Modulator-Firmware-Description_25Jan11_Rel1.pdf

VHDL Modulator Implementation Quick Start
VHDL-Modulator-Implementation-QuickRef_CKT_25Jan11_Rel1.pdf

Modulator Example Implementation
Modulator-Example-Implementation_CKT_25Jan11_Rel1.pdf

HW/SW Interface

Modulator Hardware-Software Interface Spec
Modulator-Hardware-Software-Interface-Spec_25Jan11_Rel1.pdf

Modulator Hardware-Software Interface Quick Start
Modulator-Hardware-Software-Interface-QuickRef_CKT_25Jan11_Rel1.pdf

Open Core Protocol (OCP) Profiles
Open-Core-Protocol-Profiles_CKT_25Jan11_Rel1.pdf

Software

WaCoM Software
Waveform_Software_25Jan11_Rel1.zip

WaCoM Modulator Library Programmer's Guide
WaCoM-Modulator-Library-Programmers-Guide_25Jan11_Rel1.pdf

WaCoM Modulator Library Reference
WaCoM-Modulator-Library-Reference_25Jan11_Rel1.pdf

WaCom Software Overview
WaCoM-Software-Overview_TAB_25Jan11_Rel1.pdf

Waveform Test

Test & Support [11010]

Test Vectors
Included in Waveform_VHDL_25Jan11_Rel1.tar.gz

Modulator Test Plan
Modulator-Test-Plan_25Jan11_Rel1.pdf

Laboratory Test Platforms
Laboratory-Test-Platforms_JTD_25Jan11_Rel1.pdf

Release and Support Plan
Release-and-Support-Plan_TAB_25Jan11_Rel1.pdf

It takes more than just good coding to make a waveform portable.

Legend

Document

Presentation

Actual filenames include the prefix "ESC-HDRAT-MIT-LL_" which has been removed from the filenames listed here for ease of reference.

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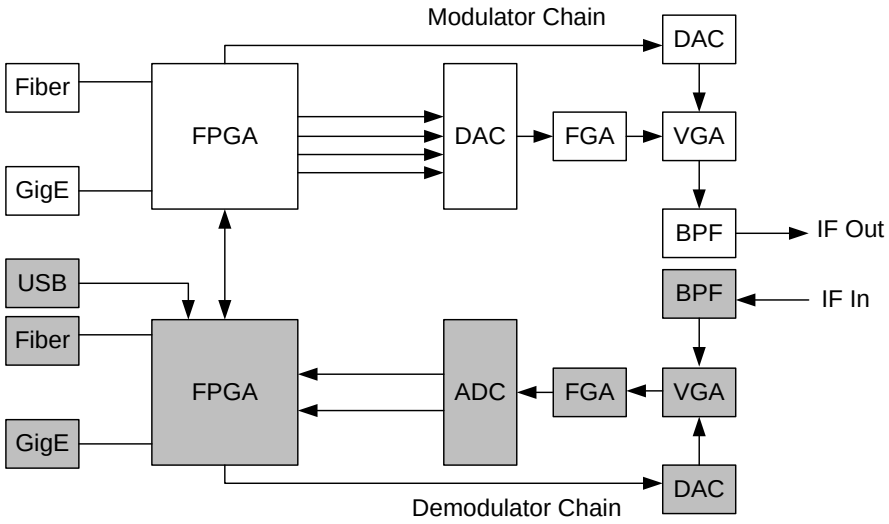
NRL's Basic Digital Radio

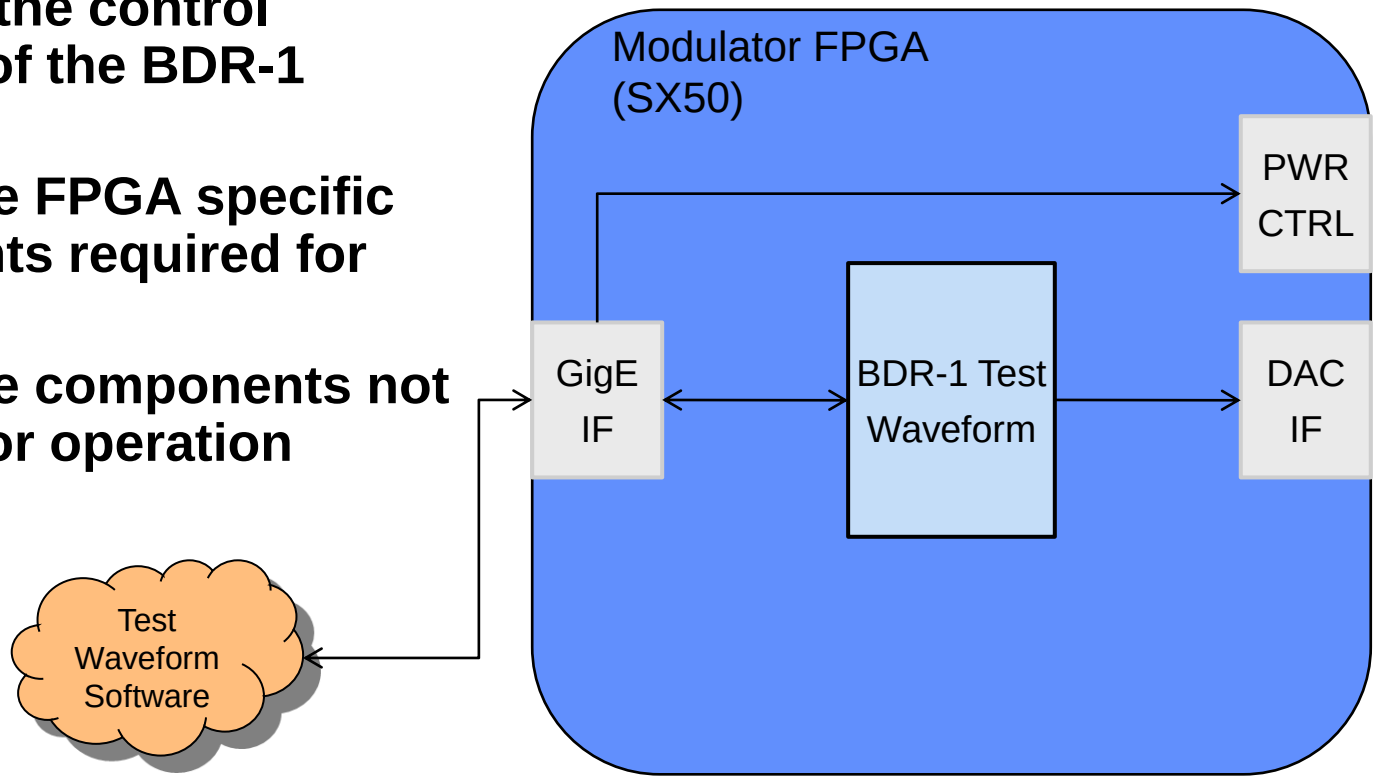
FPGAs	2 Virtex 5 SX50T
Bandwidth	~300 MHz
Sample Rate	1.75 GHz
Supported Waveforms	•NRL Test WF •HDR DVB-S2 Mod.
Dimensions	4"x7"

- **Small form factor SDR platform**
- **Low jitter VCOs for precision signal sampling/generation**
- **Preexisting GigE control and data plane, with drivers**
- **Direct L-band output elliminates need for analog additional up/down conversion stages**



HDR DVB-S2 Port to the BDR-1 Step 1

- **Ascertain the control structure of the BDR-1 platform**
- **Identify the FPGA specific components required for operation**
- **Identify the components not required for operation**



It is easier to reuse platform specific modules.

HDR DVB-S2 Port to the BDR-1 Step 1

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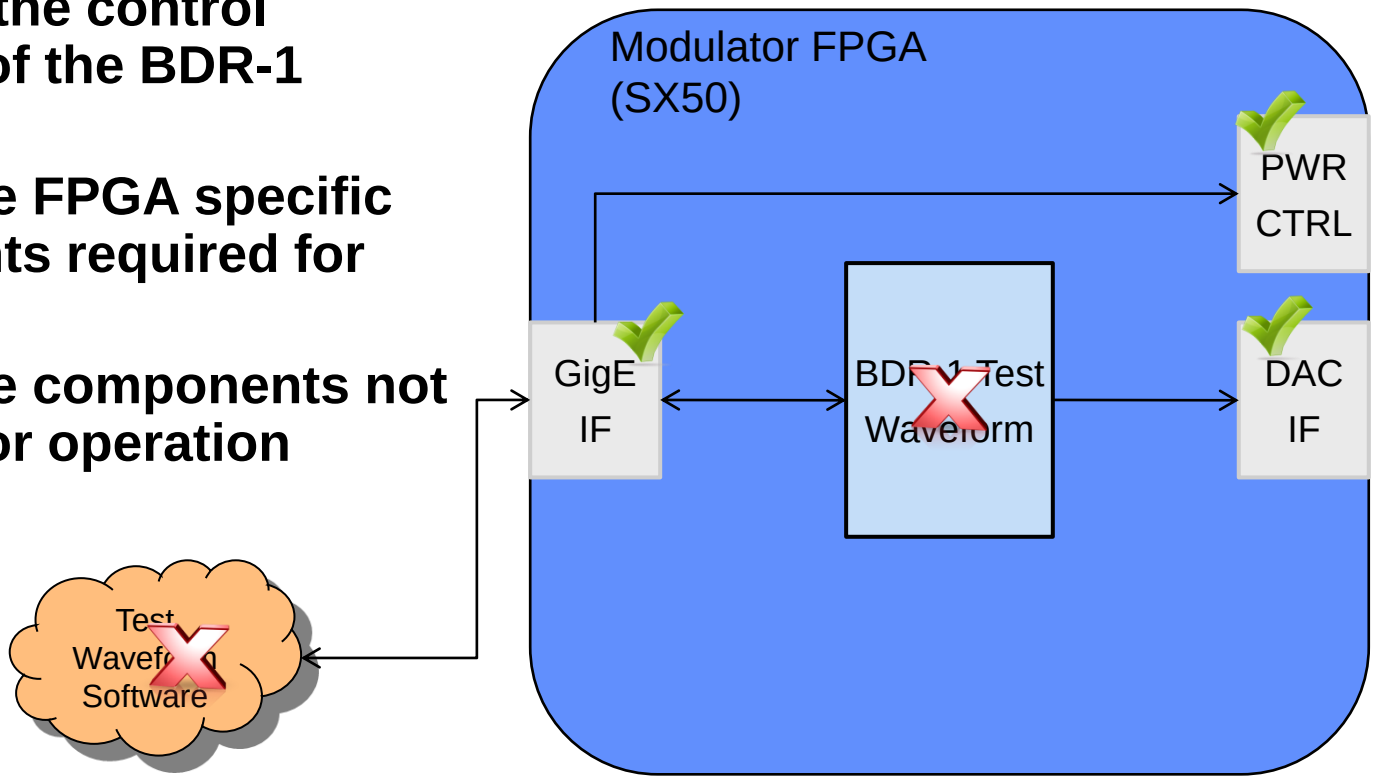
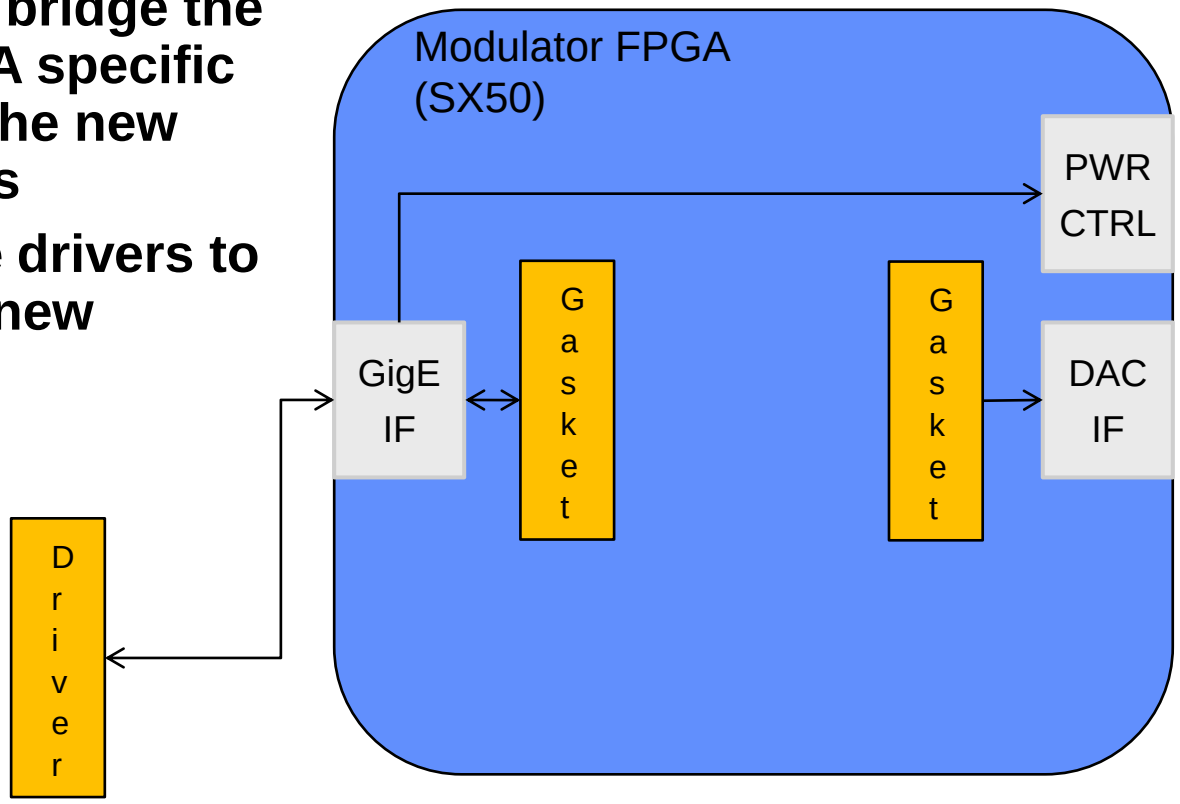


It is easier to reuse platform specific modules.

HDR DVB-S2 Port to the BDR-1 Step 2

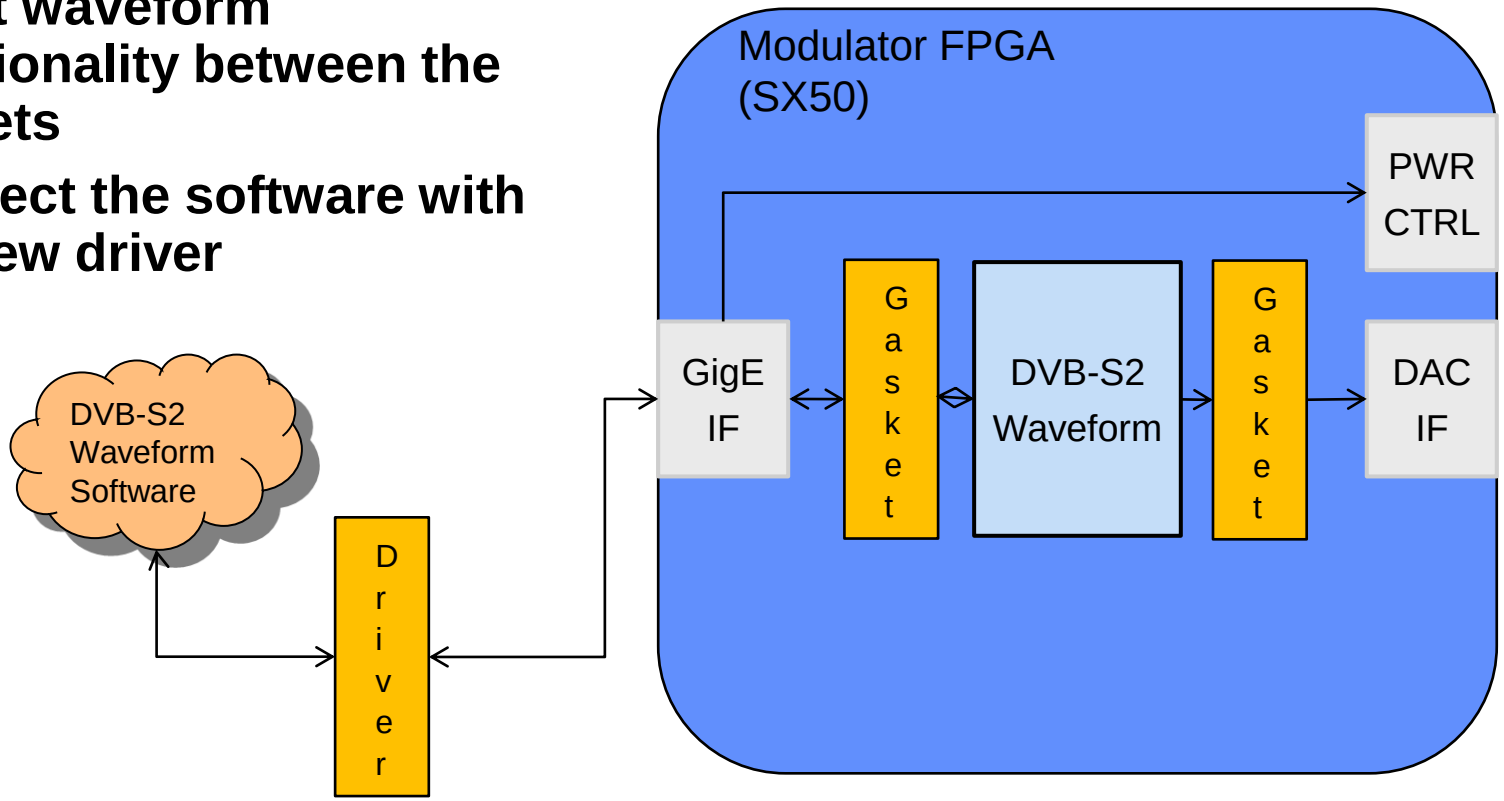
- Create *Gaskets* to bridge the gap between FPGA specific components and the new waveform modules
- Generate software drivers to interface with the new platform



Gaskets reduce configuration management issues by not changing the platform specific and or waveform specific features during a porting effort.

HDR DVB-S2 Port to the BDR-1 Step 3

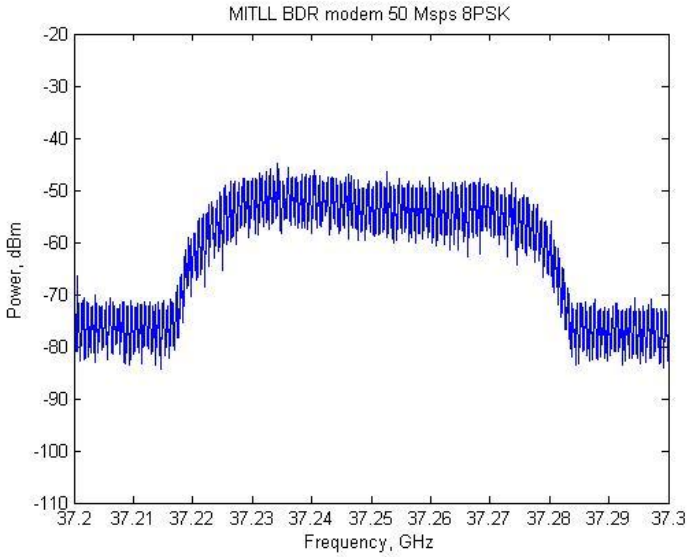
- **Insert waveform functionality between the gaskets**
- **Connect the software with the new driver**



The modulator core VHDL was not modified to support the BDR-1 platform. All new code was limited to the gaskets.

Porting Results

- 1st Successful port of HDR DVB-S2 modulator
- BDR-1 FPGA is ~1/2 the size of original development FPGA
- Demonstrated compatibility with multiple commercial DVB-S2 modems (Newtec, ECC's HI-BEAM, Avtec's HDRM, etc.)



Modem	Symbol Rate
Newtec AZ410	45 Msym/s
HIBEAM Phase 1	50 Msym/s
HIBEAM Phase 2	200 Msym/s
HDRM	218 Msym/s

Platform	BDR-1	Reference
Registers	26k	21k
LUTs	22k	20k
BRAMs	122	111
DSP48s	20	20

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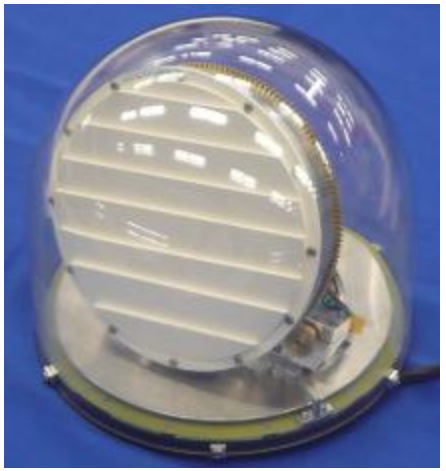
Over the Air Demonstrations of the BDR-1

- During the weeks of June 6, 2011 & June 13, 2011 the Naval Research Laboratory (NRL) conducted experiments with their Tactical Reach-back Extended Communications (TREC) system.
  - Air to ground line-of-sight (LOS) mobile system
  - Included the use of the HDR DVB-S2 waveform on the BDR-1
  - Used low power small apertures to demonstration 100's of Mbps over 10's of nautical miles @ Ka-Band

Airborne Terminal

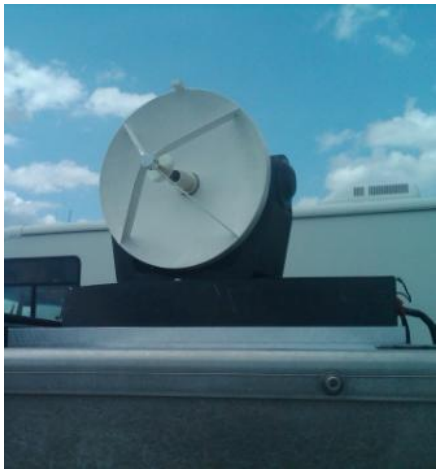
Aircraft	Cessna 210
Antenna	Risley Prism (<6.7” Height & < 5.5 lbs)
Power Amplifier	0.5 Watts @ 37.0 to 38.5 GHz
Transceiver	L-band block conversion
Modems	BDR-1 (HDR Waveform) HI-BEAM Phase 2 (DVB-S2) STD-CDL



- Aircraft altitude for testing was ~15k feet MSL
- UHF LOS used to pass telemetry data for antenna pointing
- Flight path logged via GPS for further analysis

Ground Terminal

Vehicle	HMWV (stationary)
Antenna	15” Cassegrain Antenna
Power Amplifier	0.5 Watts @ 37.0 to 38.5 GHz
Transceiver	L-band block conversion
Modems	Newtec AZ410 (DVB-S2) HI-BEAM Phase 2 (DVB-S2) STD-CDL

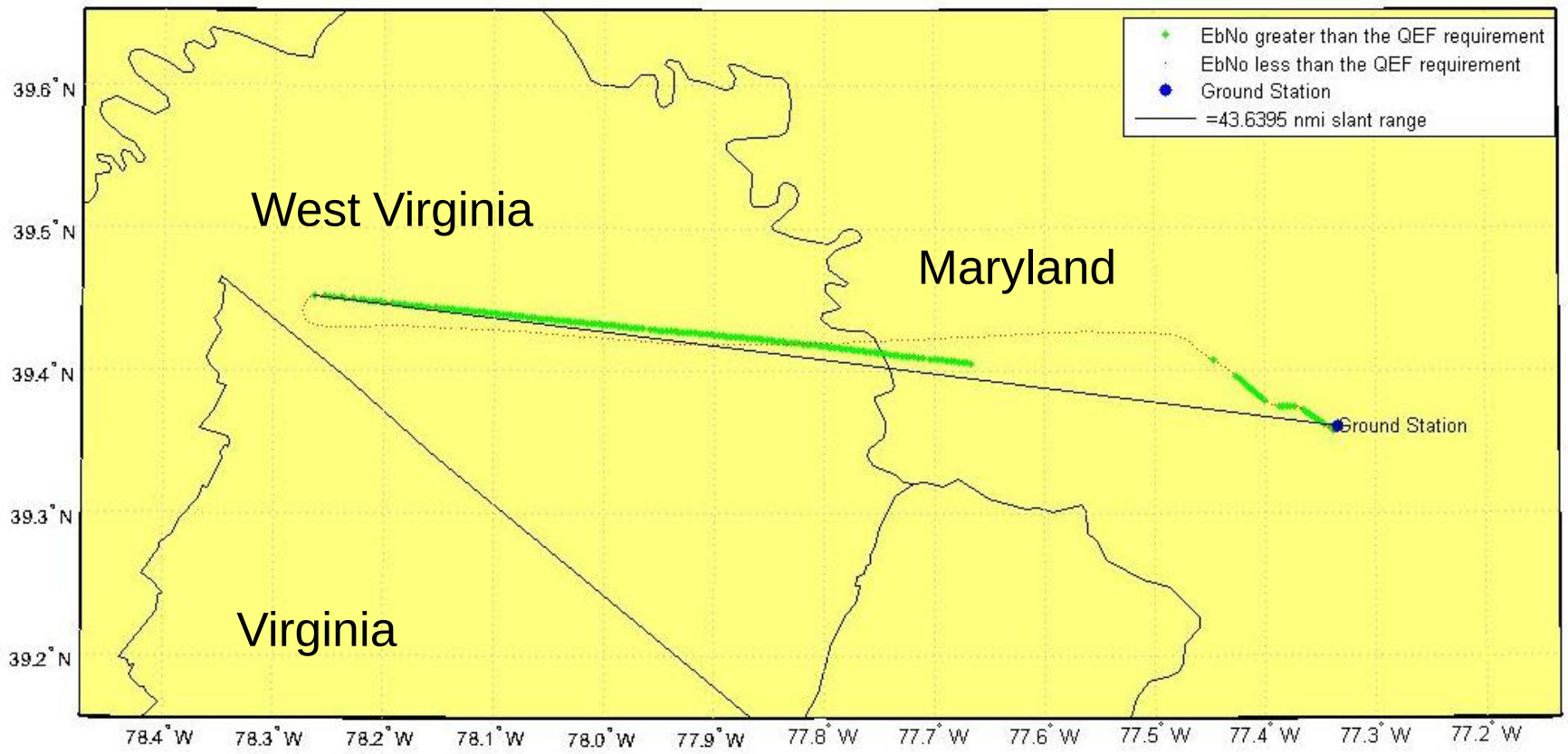


- Ground terminal was stationary for the testing
- UHF LOS used to pass telemetry data for antenna pointing
- Instrumented to collect data from the modems and GPS

Over-the-Air Test 1 10 June 2011

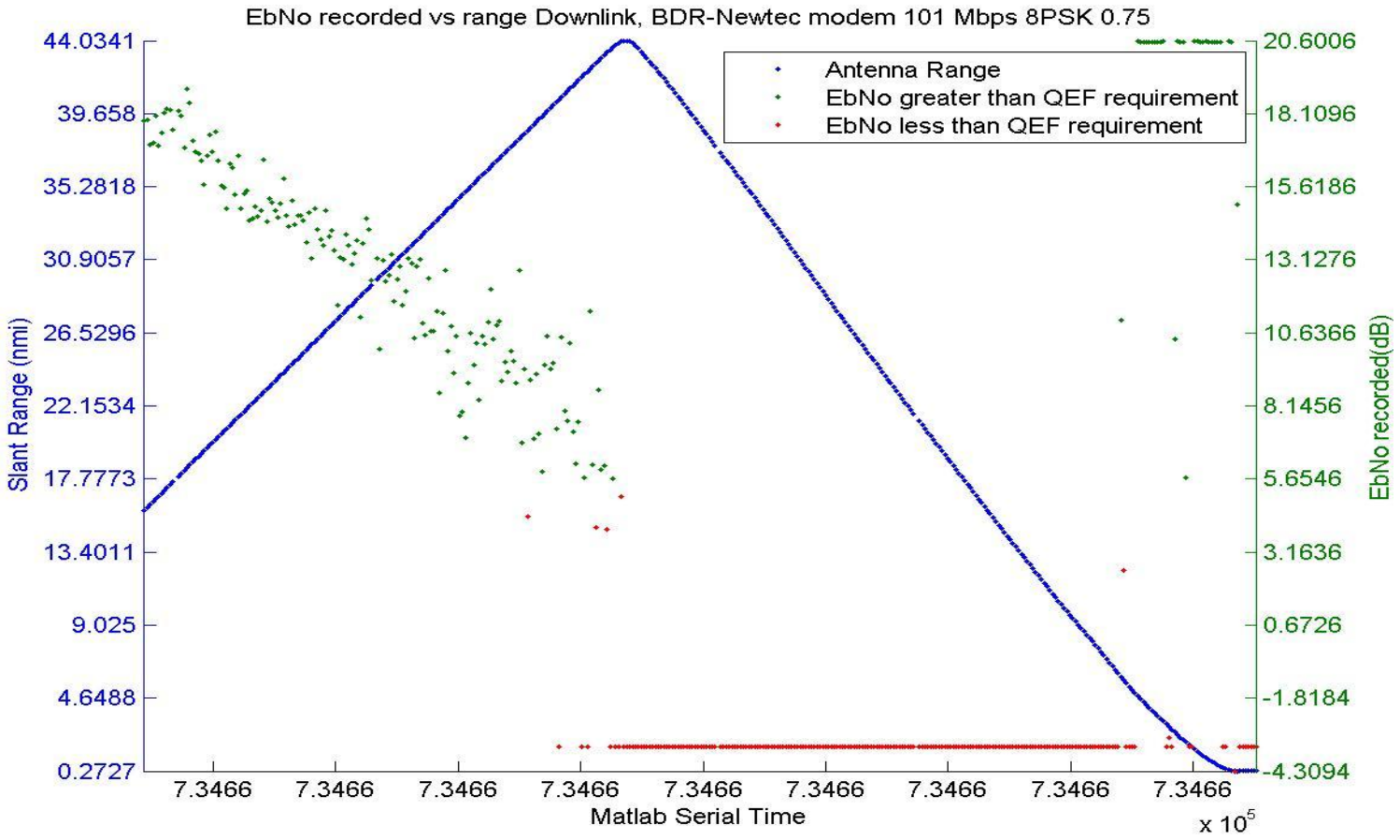
- BDR-1 in the air, Newtec Azimuth on the ground
  - Modulation settings:
    - 45 Mbaud, 101 Mbps, 8PSK, ¾
    - PRBS enabled
    - Pilots off
    - Downlink: 37.1 GHz, Uplink: 38.0 GHz
- Atmospheric conditions
  - Temperature 93 degrees F
  - Humidity 30 %

Map of E_b/N_0 Recorded during Test 1



*This slant range listed in the legend is the longest slant range at which the EbNo recorded was great enough to demodulate Quasi Error Free (QEF)

E_b/N_0 Recorded vs Range during Test 1

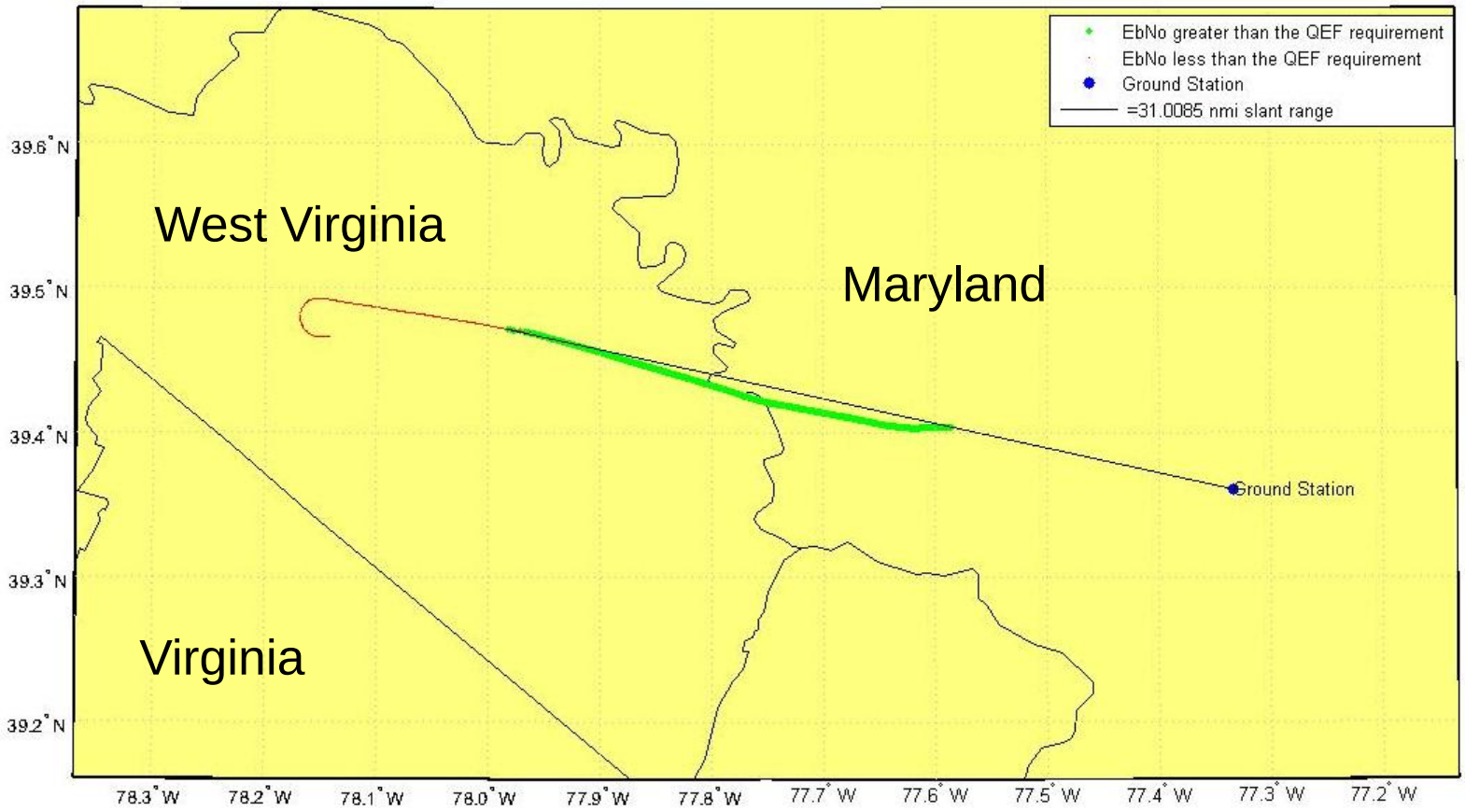


*Note this was the final test of the day and on the inbound leg the aircraft was descending in preparation to land

Over-the-Air Test 2 14 June 2011

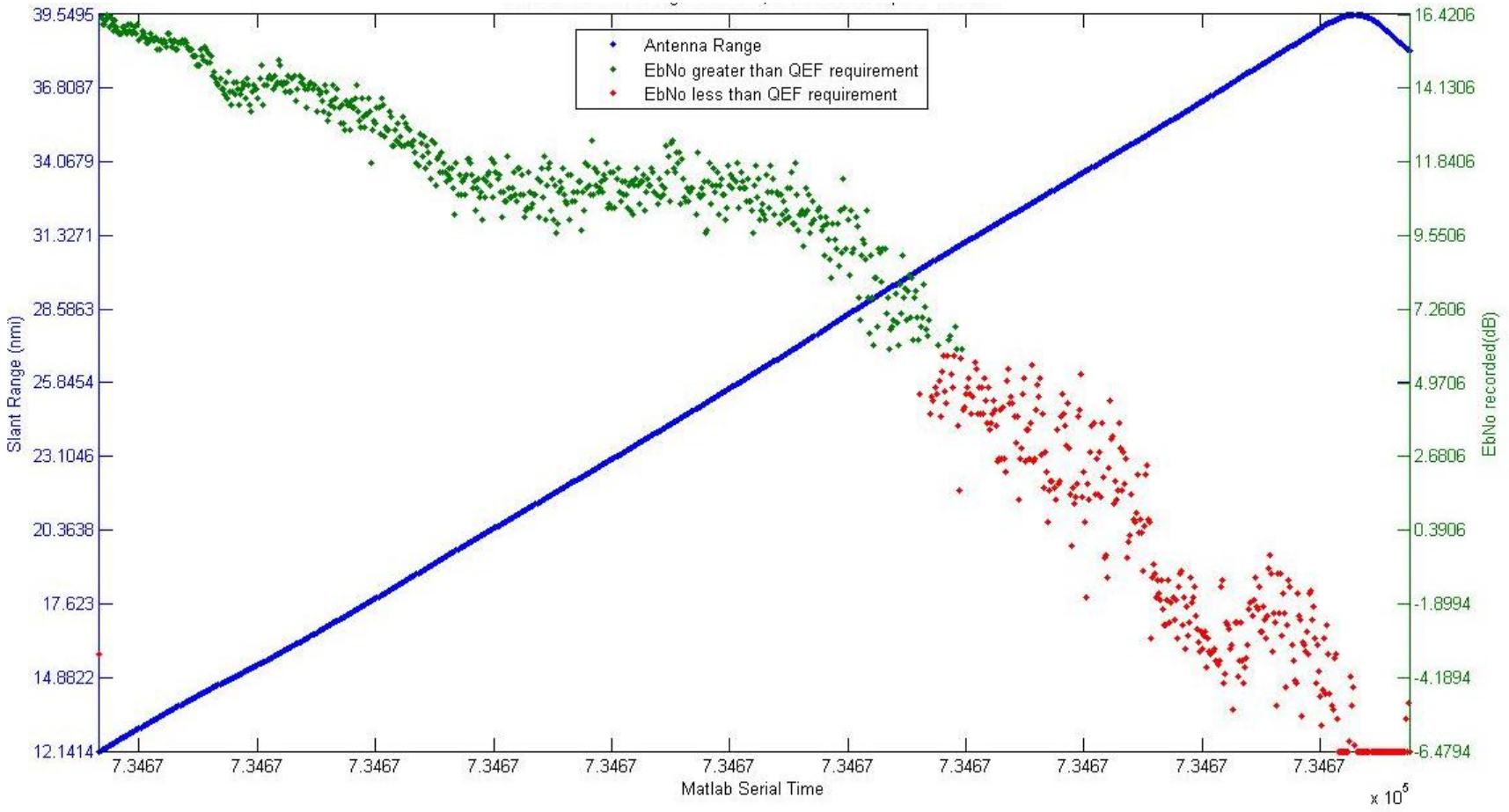
- BDR-1 in the air, ECC P2 HIBEAM modem on the ground
  - Modulation settings:
    - 134 Mbaud, 300 Mbps, 8PSK, ¾
    - PRBS enabled
    - Pilots on
    - Downlink: 37.1 GHz, Uplink: 38.0 GHz
- Atmospheric conditions
  - Temperature 75 degrees F
  - Humidity 38 %

Map of E_b/N_0 Recorded during Test 2



*This slant range listed in the legend is the longest slant range at which the EbNo recorded was great enough to demodulate Quasi Error Free (QEF)

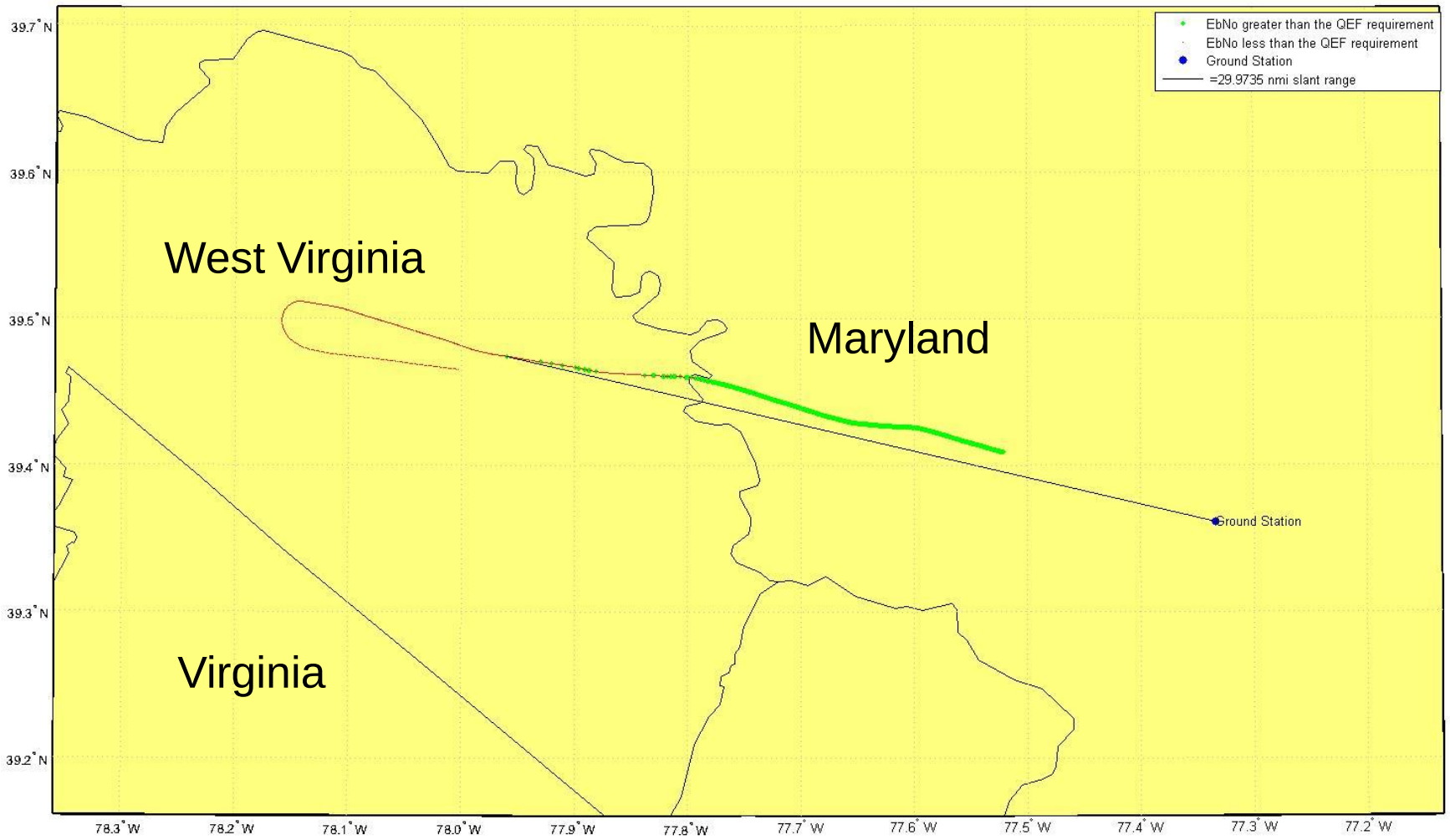
E_b/N_0 Recorded vs Range during Test 2



Over-the-Air Test 3 14 June 2011

- BDR-1 in the air, ECC P2 HIBEAM modem on the ground
  - Modulation settings:
    - 200 Mbaud, 540 Mbps, 8PSK, 9/10
    - PRBS enabled
    - Pilots on
    - Downlink: 37.1 GHz, Uplink: 38.0 GHz
- Atmospheric conditions
  - Temperature 75 degrees F
  - Humidity 38 %

Map of EbNo Recorded during Test 3



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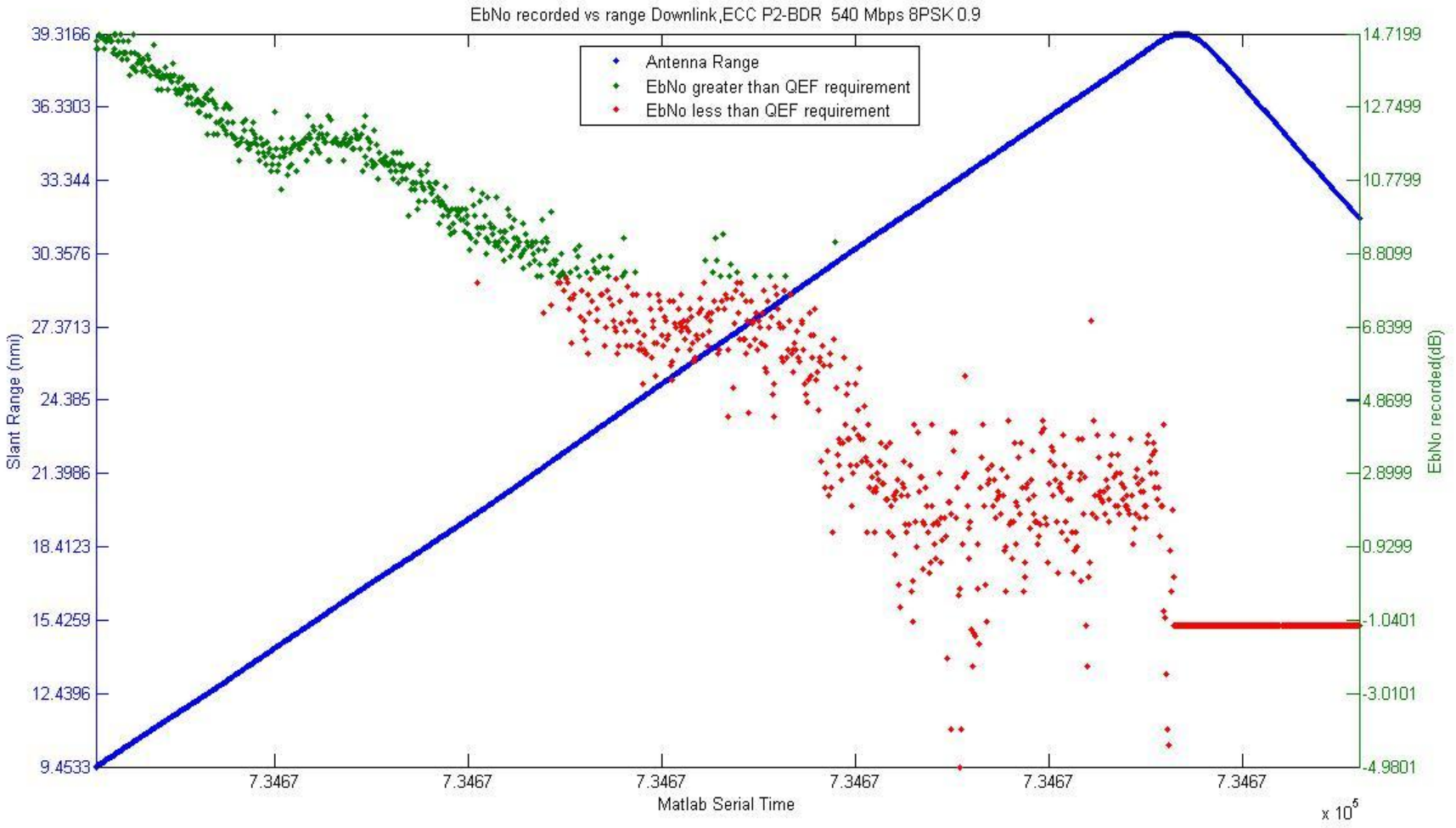
E_b/N_0 Recorded vs Range during Test 3



Over the Air Testing Results

Mode	Symbol Rate (Mbaud)	Data Rate (Mbps)	Slant Range (nmi)*	Receiver
8PSK, 3/4	45	101	35	Newtec AZ410
8PSK, 3/4	134	300	30	HI-BEAM P2
8PSK, 9/10	200	540	22	HI-BEAM P2

*This value corresponds to the furthest distance at which continuous communications were maintained.

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Conclusion

- The porting effort was straight forward and successful
  - Less than a one man month for VHDL port
- There was a high level of software reuse
- Line of sight testing showed robustness of the modulator design and platform
- Interoperability of the waveform demonstrated the level of maturity of the DVB-S2 standard in industry