LOW COST EXPERIMENTAL SOFTWARE DEFINED RADIO SYSTEM

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ABSTRACT

This paper documents the design of a low cost experimental SDR Platform as a research tool. In order to keep costs to a minimum and provide the maximum flexibility a processor-less architecture is chosen. All signal processing is carried out using a standard notebook computer.

The platform consists of four hardware elements. These are baseband transmitter board, baseband receiver board, RF transmitter board and RF receiver board. The baseband transmitter board consists of a USB 2.0 interface and two 16-bit DACs. The baseband receiver board consists of a USB 2.0 interface and two 16-bit ADCs. The transmitter RF board consists of a direct conversion modulator, local oscillator, variable gain RF amplifier and power amplifier. The receiver board consists of a low noise amplifier, a direct conversion down-converter with gain control and a local oscillator.

1. INTRODUCTION

SDR (Software Defined Radio) has begun to move from the experimental idea stage to implementation in the last number of years. To this end several groups have begun the development of various hardware platforms. Just some of these are the KUAR [1] platform from the University of Kansas and the GNU radio USRP platform [2]. While both of these are capable platforms the associated cost per unit remains high with the result that experimentation with large numbers of nodes remains out of reach. The platform documented here addresses this issue. It is specifically designed to meet high RF standards while also maintaining a low per unit cost. This is achieved in part by using components common to the mobile phone industry and relying on a personal computer to implement the signal processing element in on a general purpose CPU negating the need for expensive embedded DSPs or FPGAs.

The SDR (Software Defined Radio) hardware documented in this paper is under development at the Institute of Microelectronics and Wireless Systems at the National University of Ireland, Maynooth as part of a wider effort in SDR carried out as part of the CTVR (Center for Telecommunications Value Chain Research). It is aimed at producing a low cost, highly configurable platform that may be used to carry out experimentation in to both the best solution to the hardware software partitioning problem in such a system and also the possible uses for such a system. The platform consists of three elements, software, baseband hardware and RF hardware. The hardware element is designed in a modular way. In total there are five hardware modules in this platform. Four are documented in this paper. The fifth, which includes an FPGA is documented in a separate paper. This paper documents the low-cost baseband option and the RF hardware. A further paper at this conference documents the software stack for this platform.

The paper is organized as follows: section 2 documents the baseband sections, section 3 documents the RF sections and section gives some results.

2. BASEBAND SECTIONS

The SDR baseband section consists of two PCBs (Printed Circuit Board), the transmitter baseband section and the receiver baseband section. These boards are designed with a footprint of 100mm x 100mm and constructed from 2 layer standard FR4 material which helps to further reduce costs. The transmitter baseband section consists of a USB interface to the host computer, a dual high-speed DAC (Digital to Analog Converter) with reconstruction filters, and a clock generator chip to control the rate of digital to analog conversion. It also includes an I2C interface for the control of these elements and further elements of the RF transmitter section. It is designed so that the transmitter RF section plugs in to the baseband board vertically through a series of SMB connectors transferring power, the I2C control bus and the signals to be transmitted. This forms a very compact structure 100mm x 100mm x 50mm for the completed transmitter or receiver assembly.

The receiver baseband section is similarly constructed. It consists of a USB interface to the host computer, a multiplexer, two high-speed ADCs (Analogue to Digital Converter) , a clock control chip and two anti-aliasing filters. It is similarly constructed using SMB connectors to transfer the power, I2C and received signals between the baseband section and RF section. By using industry standard interfaces such as I2C the boards may be used with other equipment which follows these standards.

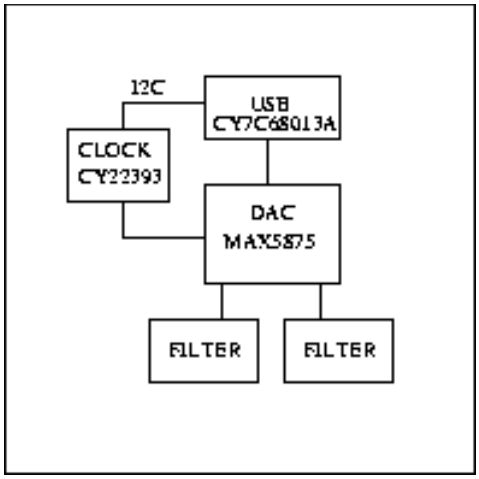

Figure 1: Transmitter baseband section

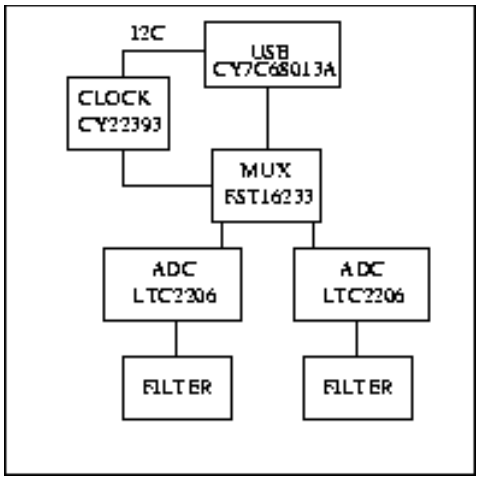

Figure 2: Receiver baseband section

It can be seen from figure 1 and figure 2 that the baseband elements contain no processing element in the data stream. An 8051 micro-controller contained in the USB IC is used to implement the I2C interface and configure the USB interface but all other signal processing is carried out on the host PC. This contributes to a considerable reduction in cost and a simpler user interface.

The platform has a maximum digital conversion rate of 80MSps in both ADC and DACs. The number of bits required was found to be 8-bits at full scale deflection for a 10 sub-channel 256QAM OFDM signal. 16-bit devices were chosen to allow a further 48dB of dynamic range to provide the maximum flexibility in the platform. With such a high conversion rate available to the platform the limiting factor is the USB interface and subsequent software.

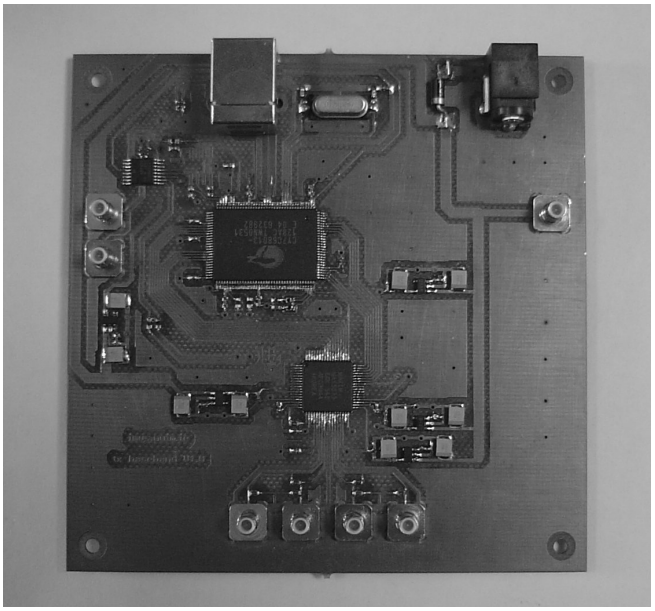

Figure 3: Photograph of transmitter baseband section

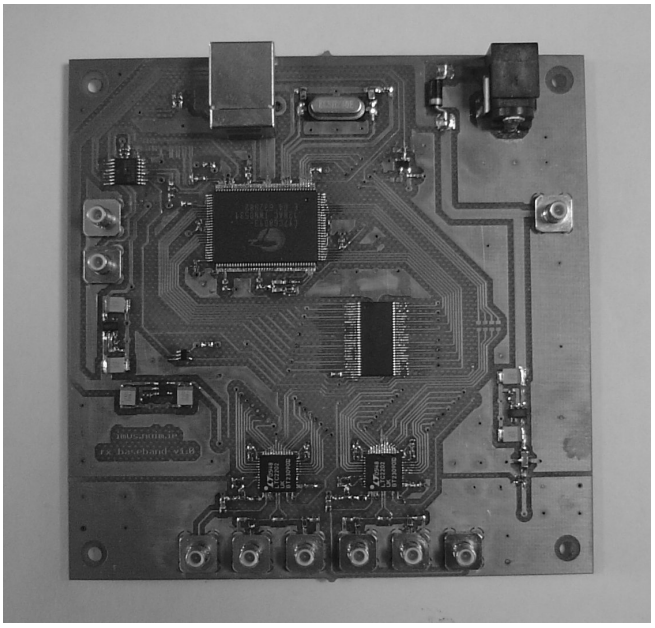

Illustration 1: Figure 4: Photograph of receiver baseband section

3. RF SECTIONS

The RF transmitter and receiver consist of a further two PCB's. These are 4 layer PCBs constructed using Rogers RO4350 substrate to ensure good RF properties. The transmitter consists of an IQ direct conversion mixer fed from a software controlled LO (Local Oscillator). The output from the mixer is fed into a variable gain RF amplifier which in turn feeds a RF power amplifier. The variable gain amplifier is controlled by an 8 bit DAC accessed over the I2C bus. The LO is controlled through an SPI to I2C bridge again controlled over the I2C bus. In this way the transmit center frequency can be configured through software with 256 levels of output power control available also under full software control.

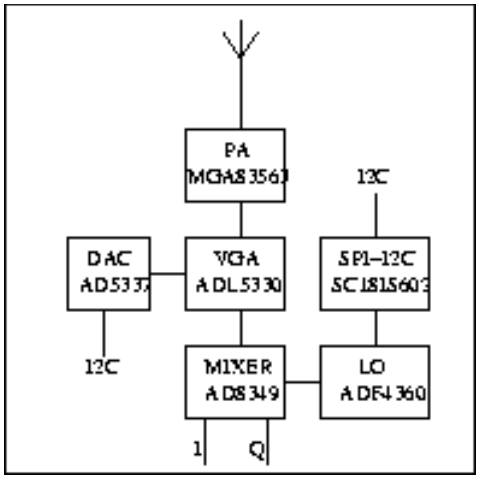

Figure 5: Transmitter RF section

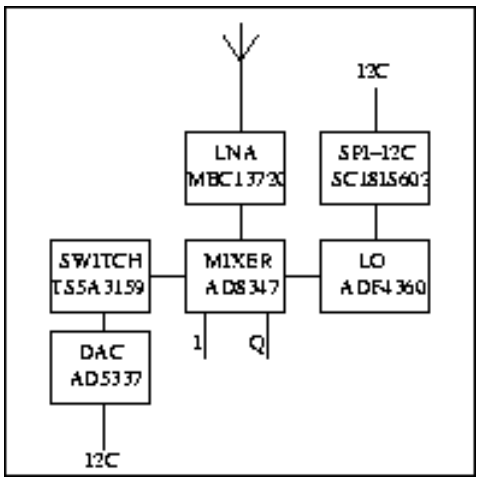

Figure 6: Receiver RF section

The receiver is similarly constructed. It consists of a LNA followed by a direct conversion IQ mixer. The AGC (Automatic Gain Control) of the mixer section may be selected through software as either hardwired or driven through software. This is achieved through an 8-bit DAC and analog switch connected to the I2C bus. The LO is again controlled through an SPI to I2C bridge over the I2C bus.

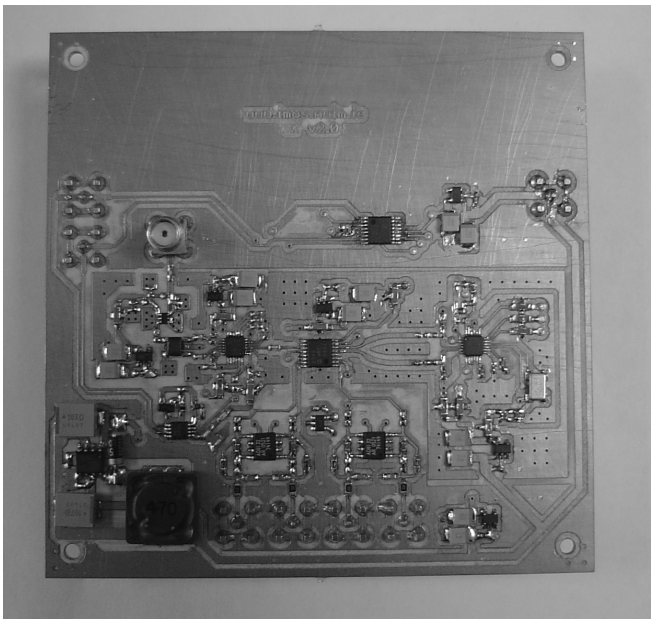

Figure 7: Photograph of transmitter RF section

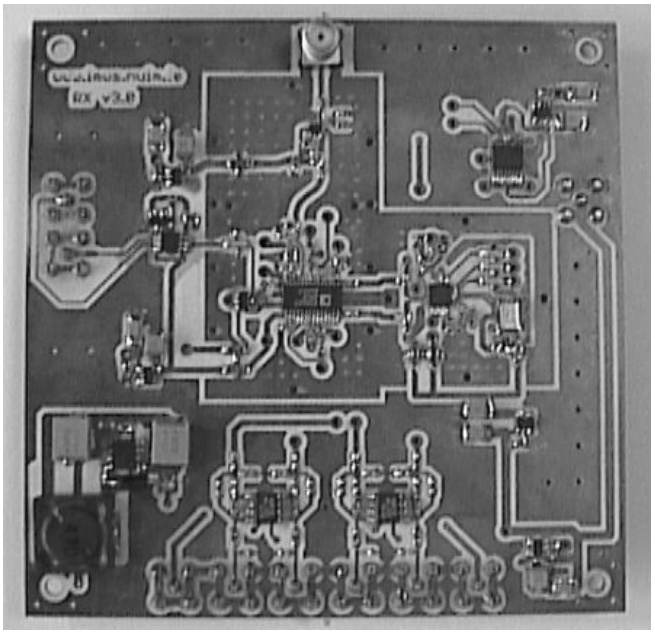

Figure 8: Photograph of the receiver rf section

Thus, the RF system supports up to 40MHz of channel bandwidth, 24 dBm of transmit output power, -104dBm receive sensitivity, -152 dBc/Hz phase noise and -0.87dBm receiver IIP3. This is much greater than the continuous transmit capability of the USB interface.

4. SOFTWARE

The software element of the system has three parts. These are a driver, embedded code, and signal processing functions. These are briefly described here, as they are documented in greater detail in an additional paper here.

A USB driver has been written in the 'c' programming language as a kernel module to the popular Linux operating system. This forms the interface between the PC and the hardware.

Embedded code running on the 8051 micro-controller in the USB interface chip implements the control interface between the PC and the I2C bus.

Finally software written in 'c' to implement various signal processing fuctions such as filtering has been developed.

5. RESULTS

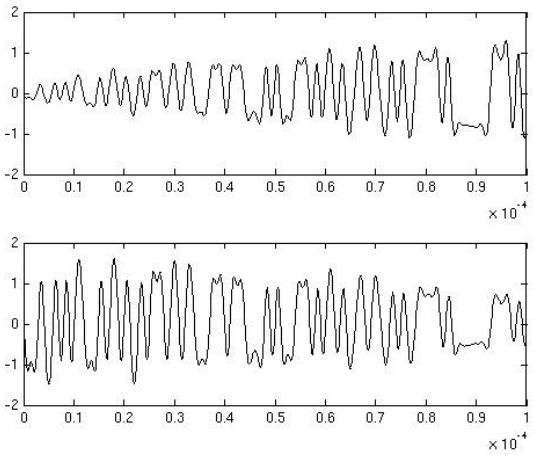

Figure 10: received BPSK signal

Some results are shown for the receiver section below. The trasmitter was configured to transmit a BPSK signal at 1Mbps with a root raised cosine signal shape with rolloff of 0.5. Figure 9 shows a plot of the receiver signal at baseband before digitization. The characteristic pulse shape can clearly be seen. Figure 10 shows an eye diagram generated in MATLAB after timing and carrier recovery. A clear opening can be seen in the eye diagram showing good SNR properties.

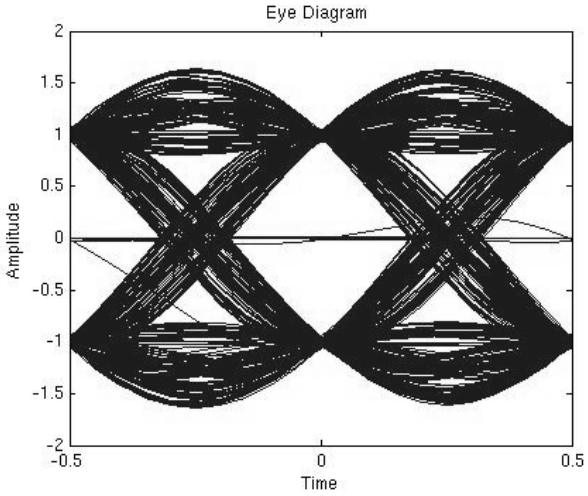

Figure 11: Eye diagram for BPSK signal

6. CONCLUSIONS

This paper has presented a low cost experimental SDR platform. The platform uses off the shelf components through out the design, focusing on a direct conversion architecture.

7. ACKNOWLEDGMENTS

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3. REFERENCES

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[2] http://www.comsec.com/wiki/?Universal SoftwareRadioPeripheral