PERFORMANCE ANALYSIS OF A TIME-INTERLEAVED SAMPLING ARCHITECTURE FOR A SOFTWARE DEFINED ULTRA WIDEBAND RECEIVER

Christopher R. Anderson and Jeffrey H. Reed

Mobile and Portable Radio Research Group
Virginia Polytechnic Institute and State University
Blacksburg, VA
{chanders, reedjh}@vt.edu

ABSTRACT

A Software Defined Radio for Ultra Wideband (UWB) communication systems places several stringent requirements on the Analog to Digital Converter (ADC). The ADC must have a sufficiently fast sampling frequency and SNR to accurately reconstruct the received UWB pulse. Such an ADC can be prohibitively expensive, as well as challenging to interface with a DSP or FPGA.

An alternative approach is to sample the received signal with multiple slower ADCs operating on interleaved sampling clocks. Such a system operates as if it were a single ADC operating at a much higher sampling rate; however, gain, offset, and timing mismatches can significantly degrade the overall system performance. This paper presents simulation results for UWB pulses sampled using an 8-ADC Time Interleaved Sampling architecture running at an aggregate sampling rate of 8 GS/s. The results indicate that the performance of the system is primarily constrained by ADC gain and timing mismatches.

1. INTRODUCTION

Software Defined Radios (SDR) have the potential of changing the fundamental usage model of wireless communications devices, but the capabilities of these transceivers are often limited by the speed of the underlying ADCs, DSPs, and FPGAs. A SDR UWB receiver provides tremendous flexibility and rapid prototyping capabilities over a fixed hardware implementation [1]. Such a receiver has the capability of supporting multiple data rates, modulation or multiple access schemes, and can adapt to the propagation environment. Currently, state-of-the-art UWB communication systems are composed of custom-developed hardware, and do not use SDR architectures. Several major challenges are involved in developing such a communication testbed—extremely high sampling rates, huge amounts of input/output data, and a tremendous amount of digital processing power. These challenges are particularly daunting when Commercially available Off-The-Shelf (COTS) components are used in the development of such a system. For example, accurately reconstructing a 500 picosecond UWB pulse requires a sampling frequency of at least 8 GHz. Because using a single 8 GS/s ADC would be extremely expensive, the following alternative techniques have been discussed in the literature:

- Equivalent Time Sampling [2, 3] where multiple UWB pulses are transmitted per data bit. At the receiver, an ADC running at a low sampling frequency samples each received pulse at a slightly different point in time. These samples can then be combined to reconstruct an approximation of the received signal.
- Frequency Domain Sampling [4] where the received UWB pulse is passed through a filter bank and separated into a number of different spectral regions. An ADC in each spectral region is able to determine the amount of energy present in that region. An IFFT operation can then be used to reconstruct the received signal.
- Time-Interleaved Sampling (TI Sampling)—where multiple ADCs sample the received signal at different points in time in a round-robin fashion—can be used to achieve the target sampling frequency [1, 5, 6]. The ADC sampling clocks are offset from each other by a specific amount, so that each ADC samples the received pulse at a slightly different point in time, as illustrated in Figure 1. The samples can then be combined to reconstruct the received signal.

Both Equivalent Time Sampling and Frequency Domain sampling systems have significant disadvantages. An Equivalent Time Sampling receiver is restricted to transmitting multiple UWB pulses per data bit, thus, the data rate will always be lower than the pulse rate. The Frequency Domain Sampling receiver allows the transmission of one

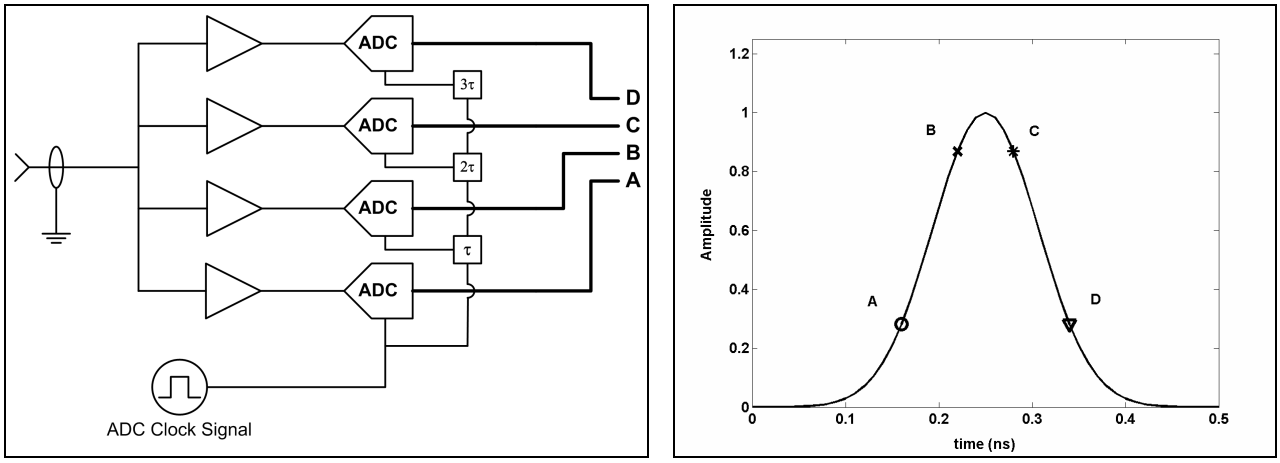


Figure 1: (a) TI-Sampling Illustrated using four ADCs. The first ADC samples the received signal at Point A, the second at Point B, the third at Point C, and the fourth at Point D. (b) The FPGA is then able to reconstruct the received signal as if it were sampled by a single ADC, from [7].

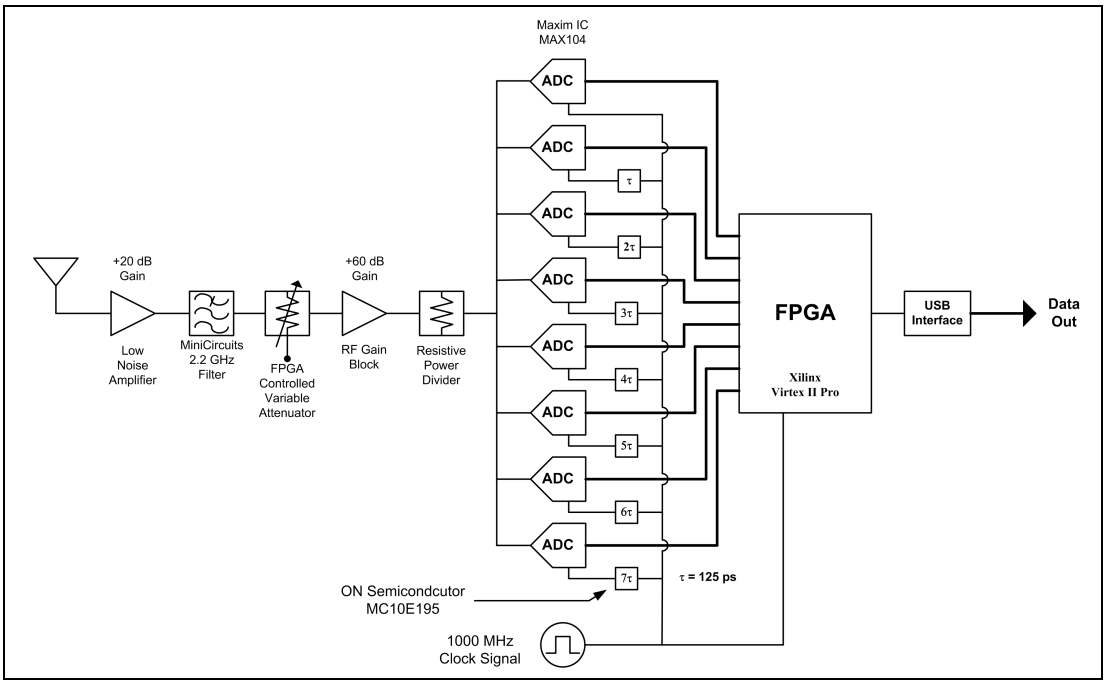


Figure 2: A block diagram of the UWB SDR receiver.

UWB pulse per data bit, but requires a high-quality analog filter bank, as well as devoting processing resources to performing the IFFT operation.

The TI Sampling receiver combines the best aspects of both receivers—the use of lower speed/lower cost ADCs to sample the received signal along with the ability to transmit one data bit per UWB pulse. Additionally, the TI Sampling receiver operates as if it used a single ADC operating at *N* times the individual ADC sampling rate (where *N* is the number of ADCs). Therefore, the effective sampling frequency of the receiver can be described by the following equation:

$$f_{S_{Effective}} = Nf_S \tag{1}$$

Where $f_{S_{Effective}}$ is the effective sampling frequency, N is the number of ADCs, and f_S is the sampling frequency of an individual ADC. The TI Sampling receiver does, however, suffer from performance degradation due to timing, gain, and offset mismatches between ADCs.

2. OVERVIEW OF THE RECEIVER ARCHITECTURE

A basic block diagram of the receiver is given in Figure 2, and a detailed description is contained in [1]. Essentially, the receiver consists of an analog RF front end, the ADC and clock distribution bank, the FPGA, and a USB 2.0 interface device. The RF front end utilizes several ultra-broadband amplifiers, attenuators, and filters and feeds the received signal to the ADCs. A thorough discussion of the details of the RF front end is, however, beyond the scope of this paper. A bank of eight Maxim IC MAX104 ADCs is used to sample the input analog signal. The samples are then sent to a Xilinx VirtexII-Pro FPGA for digital processing. For a target 100 Mbps data rate, UWB pulses are transmitted once every 10ns. To achieve the target data rate, the system is assumbed to be operating in a very short range, line-of-sight channel with minimal multipath.

The MAX104 ADCs have an analog input bandwidth of 2.2 GHz, and therefore, the transmitted UWB pulse duration was chosen at 500 picoseconds. The MAX104 ADCs also have a maximum sampling frequency of 1 GHz, and 8 bits of quantization. Accurately reconstructing the transmitted pulse in the digital domain requires a sampling rate of 8 GHz, and therefore, the ADC bank consists of eight ADCs, each operating at a 1 GHz sampling frequency. At the target data rate (100 Mbps), an 8 GHz sampling rate results in exactly 80 samples per UWB pulse.

As discussed previously, the performance of a TI Sampling architecture is highly dependent on matching the individual ADC gains, offsets, and timing delays [8]. Mismatches may result in a significant distortion of the received signal, which can be thought of as noise added to the ideal received signal by the TI Sampling process. Thus, it is possible to define a Signal-to-Noise-Ratio (SNR) which quantifies how much noise is added to a received UWB pulse by TI Sampling as compared to sampling with a single ADC operating at the effective sampling frequency [10]:

$$SNR_{Effective} = 8.59 + 6.02B + 10\log_{10}\left(\frac{\tau}{2\pi T}\right) - 10\log_{10}\left(\frac{\sum_{i=0}^{N-1} x_i^2}{\sum_{i=0}^{N-1}(x_i - y_i)^2}\right) \quad (2)$$

Where $SNR_{Effective}$ the Effective SNR of the TI-Sampling system, including both quantization noise and TI-Sampling mismatch noise (dB), B is the number of bits of quantization for an individual ADC, τ is the UWB pulse width (seconds), T is the time between successive UWB pulses (seconds), x_i is the amplitude of the i^{th} sample value for the signal sampled by a single ADC, y_i is the amplitude of the ith sample value for the signal sampled by the time-interleaved ADCs, and N is the number of samples per UWB pulse.

3. SIMULATION DESIGN

In an attempt to quantify how ADC mismatches impacted the SNR of the system, a series of simulations were performed. Three different UWB pulse widths were investigated: a 1.0 nanosecond Gaussian monocycle, a 1.5 nanosecond Gaussian monocycle, and a 2.0 nanosecond Gaussian monocycle. For each pulse width, four separate simulations were performed:

- Gain Mismatch
- Offset Mismatch
- Timing Mismatch
- Total Combined Mismatch

For each simulation, the UWB pulse had an amplitude equal to the full-scale ADC input range. The pulse rate was set at 100 Mpulses/sec, the effective sampling rate set at 8 GHz and 8 bits of quantization, which leads to 80 ADC samples per received UWB symbol. The simulation approach was a semi-analytic simulation with each of the 8 ADCs operating at an individual sampling frequency of 1 GHz. Simulation runs were governed by Equation 3, which has been adapted from [8] for use with a Gaussian Monocycle. In Equation 3, A is the amplitude of the pulse, Gi is the gain of the i^{th} ADC, T_S is the sampling time interval, equal to the inverse of the effective sampling frequency (in this simulation T_S = 125 picoseconds), δt_i is the deviation from the ideal sampling instance for the ith ADC, os_i is the offset from the ideal Input/Output characteristic for the i^{th} ADC, and m is an integer index.

For each simulation run, Gain, Offset, and Timing mismatches were allowed to vary randomly up to a pre-defined maximum allowed deviation. Twenty maximum allowable deviations were chosen as fixed percentages (0-100%) of the maximum possible Gain, Offset, and Timing mismatches for the MAX104 ADCs (±50% Gain mismatch, ±5.5 Least Significant Bit Offset mismatch, and ±125 ps timing mismatch). For every maximum allowable deviation, 25,000 UWB pulses were simulated. The resulting SNR degradation was calculated for every pulse, and the results were averaged over all 25,000 pulses.

4. SIMULATION RESULTS

4.1 Gain Mismatch Simulation

The maximum gain variation between the individual MAX 104s is specified at ± 5% [9]. However, due to non-ideal RF components, the worst-case potential mismatch was estimated at ± 50%. For simulation purposes, the nominal

$$V_{out}(n)=\begin{cases} G_1A(nT_s+\delta t_1)e^{-\frac{(nT_s+\delta t_1)^2}{2\sigma^2}}+os_1 & (n=8m) \\ G_2A(nT_s+\delta t_2)e^{-\frac{(nT_s+\delta t_2)^2}{2\sigma^2}}+os_2 & (n=8m+1) \\ G_3A(nT_s+\delta t_3)e^{-\frac{(nT_s+\delta t_3)^2}{2\sigma^2}}+os_3 & (n=8m+2) \\ G_4A(nT_s+\delta t_4)e^{-\frac{(nT_s+\delta t_4)^2}{2\sigma^2}}+os_4 & (n=8m+3) \\ G_5A(nT_s+\delta t_5)e^{-\frac{(nT_s+\delta t_5)^2}{2\sigma^2}}+os_5 & (n=8m+4) \\ G_6A(nT_s+\delta t_6)e^{-\frac{(nT_s+\delta t_6)^2}{2\sigma^2}}+os_6 & (n=8m+5) \\ G_7A(nT_s+\delta t_7)e^{-\frac{(nT_s+\delta t_7)^2}{2\sigma^2}}+os_7 & (n=8m+6) \\ G_8A(nT_s+\delta t_8)e^{-\frac{(nT_s+\delta t_8)^2}{2\sigma^2}}+os_8 & (n=8m+7) \end{cases} \quad (3)$$

gain was set at 1.0. Gain offsets were simulated from 0% variation (perfect gain matching) to ±100% allowable variation (±50% gain mismatch). Thus, for a 100% variation, the gain of an individual ADC could vary from a minimum of 0.5 to a maximum of 1.5. Gains were randomly varied for each individual UWB pulse, but remained fixed for the duration of the pulse. Simulation results are given in Figure 3a. Note that the SNR performance is independent of the pulse width, as noise introduced by gain mismatches is proportional only to the magnitude of the input signal and the amount of gain mismatch across the ADC array [10, 11]. From the figure, a 6 dB degradation in the pulse SNR occurs at ±5% variation; at ±100% variation, $SNR_{Effective}$ reduces to a minimum of about 18 dB.

4.2 Offset Mismatch Simulation

The maximum offset variation between the individual MAX 104s is specified at ±5.5 Least Significant Bits (LSBs) [9]. Offset mismatches were simulated from 0% (perfect offset matching) to ±100% variation, or ±5.5 LSBs. Simulation results are given in Figure 3b. Note that offset mismatches produce different results for different pulse widths, due to the fact that offset noise is a result of the ADC interleaving process and independent of the input signal [10, 11]. Thus, longer duration UWB pulses (which have a larger average signal power) will have a higher $SNR_{Effective}$ for offset noise. Also for offset noise, mismatch variations of less than ±15% (±1 LSB) are dominated by the quantization noise. Thus, the SNR degradation is more gradual than both gain and timing mismatches, at least until the offset noise becomes significantly larger than the quantization noise. For a single LOS signal, it takes a 20% offset variation (±1.1 LSBs) to degrade the pulse SNR by 6 dB (an $SNR_{Effective}$ of 33 - 39 dB depending on the pulse width). At the maximum possible offset mismatch, $SNR_{Effective}$ is reduced only to 22.5 - 25.5 dB.

4.3 Timing Mismatch Simulation

The timing of the ADC clocks is controlled by a series of programmable delay chips, with a delay resolution of ± 10 picoseconds. Additionally, clock jitter is introduced by every element in the clock distribution network. As the system sampling rate was set at 8 GHz (1 sample every 125 picoseconds), it was decided that the maximum permissible deviation would occur when successive samples overlapped in time. In other words, the maximum allowable timing mismatch would be ±125 picoseconds, corresponding to 2 ADCs sampling exactly the same point in the received waveform. As with the gain mismatch simulation, timing mismatches were fixed for a given simulation run, but allowed to vary randomly from one run to the next. Simulation results are shown in Figure 3c.

As seen from the figure, $SNR_{Effective}$ for timing mismatches degrades very rapidly: a ±5% (±6.25 ps) mismatch reduces the SNR by about 4 dB; a ±10% (±12.5 ps) mismatch reduces the SNR by nearly 10 dB. At ±100% mismatch, $SNR_{Effective}$ is reduced to only 12 - 17 dB. Note that SNR due to timing mismatches is dependent on the pulse width. This result is expected, as noise added by timing mismatches is proportional to the slew rate (or time derivative) of the input signal [10, 11]. A shorter time duration UWB pulse has a higher slew rate and, therefore, will experience greater noise added by the TI-Sampling process.

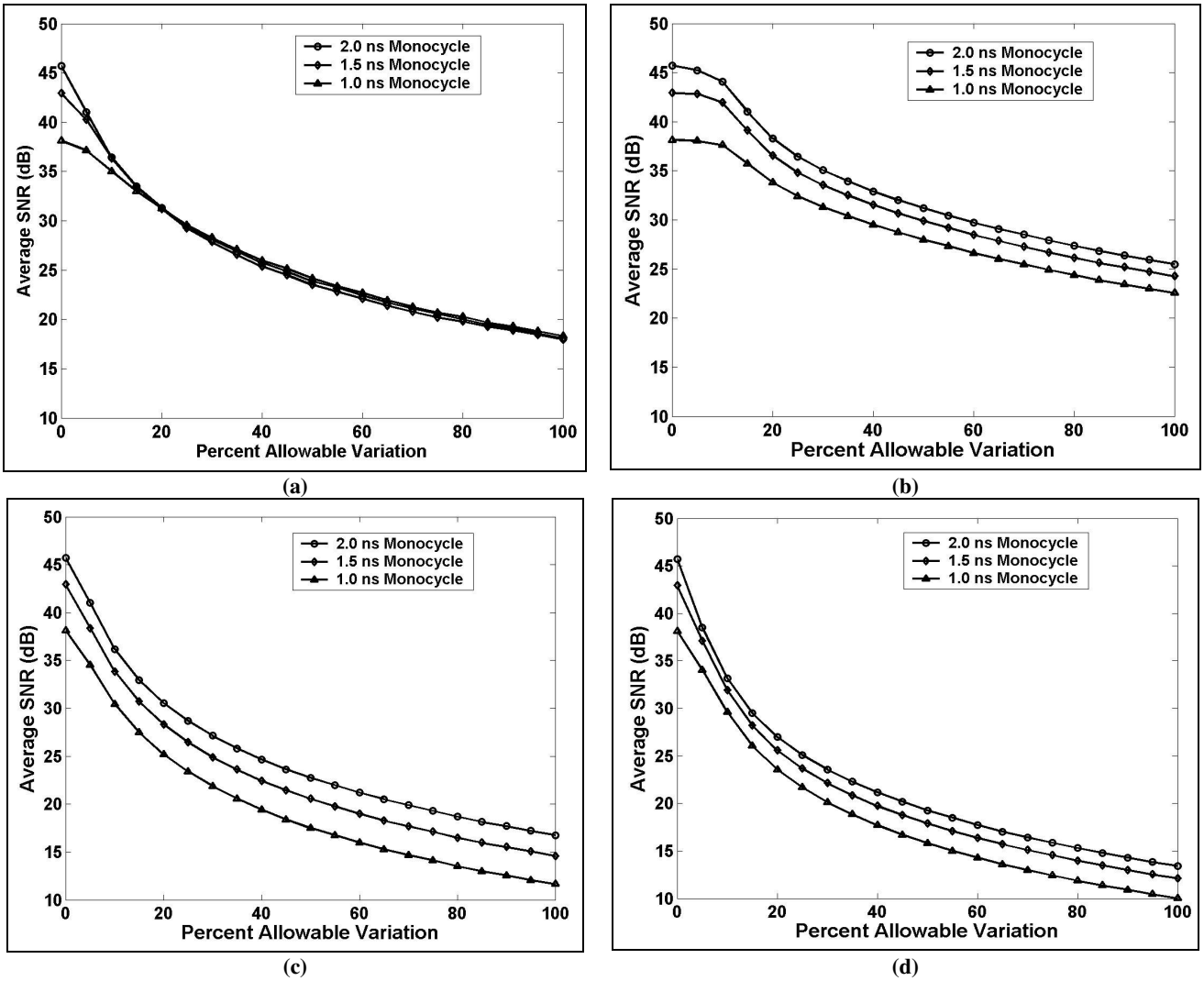


Figure 3: Performance of an 8-ADC TI-Sampling receiver. (a) Effects of gain mismatch—100% Allowable Variation is a gain mismatch of 50% (ADC gain of 1.0 ±0.5), (b) Effects of offset mismatch—100% Allowable Variation is an offset mismatch of ±5.5 LSBs, (c) Effects of timing mismatch—100% Allowable Variation is a timing mismatch of ±125 ps, and (d) Combined effects of all three mismatches (gain, offset, and timing).

4.4 Total Combined Mismatch Simulation

The total mismatch simulation was an effort to investigate the SNR degradation when the effects of Gain, Offset, and Timing Jitter mismatches were combined. The simulations were run exactly as before, with the difference that instead of varying just one component, all three were allowed to change. Mismatches were simulated from ±0% mismatch (perfect gain, offset, and timing matching) to ±100% mismatch (gain mismatch of ±50%, offset mismatch of ±5.5 LSBs, and timing mismatch of ±125 ps). Simulation results are given in Figure 3d. A 6 dB reduction in $SNR_{Effective}$ is seen for a ±5% total system variation (Gain Mismatch of ±5%, Offset Mismatch of ±0.275 LSBs, and Timing Mismatch of ±6.25 ps). At 100% mismatch, $SNR_{Effective}$ is reduced to as little as 10 - 13 dB.

5. DISCUSSION OF RESULTS

These simulation results reveal that if the individual ADC parameters can be matched to within ±5%, then the TI-Sampling receiver SNR will only be 6 dB below the SNR of a single 8 GS/s ADC. The receiver's performance is heavily dominated by both gain and timing mismatches; therefore, careful attention must be paid to matching the RF gain stages for each of the ADCs as well as ensuring a low-noise, low-jitter clock distribution network.

One technique for mitigating the effects of gain and offset mismatches is to make use of a pilot-based or transmitted reference UWB receiver, described in [7, 10, 12-14]. Essentially, a number of pilot pulses are recorded by the receiver and then averaged together to form a template for a matched filter operation. In such a pilot-based

receiver, the gain, offset, and static timing mismatches are replicated in both the pilot symbols and data symbols, potentially mitigating the overall receiver's performance degradation due to TI-Sampling mismatches.

6. CONCLUSIONS

In this paper, we have illustrated the performance of an 8 ADC Time Interleaved Sampling Ultra wideband receiver. gain and timing mismatches were shown to dominate the performance degradation of the receiver, with ±5% mismatches, resulting in a 6 dB reduction in SNR. The methodology used to simulate the receiver performance is easily applicable to other ADCs and ADC sampling bank configurations (e.g. 16 ADCs sampling at 500 MHz with 12 bits of quantization).

REFERENCES

[1] D. Agarwal, C. R. Anderson, and P. M. Athanas, "An 8 GHz ultra wideband transceiver prototyping testbed," to appear in 16th *IEEE International Workshop on Rapid System Prototyping*, June 2005.

[2] I. D. O'Donnell, M. S. W. Chen, S. B. T. Want, and R. W. Brodersen, "An integrated, low power, ultra-wideband transceiver architecture for low-rate, indoor wireless systems," *IEEE CAS Workshop on Wireless Communications and Networking*, September, 2002.

[3] P. Withington, R. Reinhardt, and R. Stanley, "Preliminary results of an ultra-wideband (impulse) scanning receiver," *IEEE MILCOM*, Atlantic City, New Jersey, November 1999, Vol. 2, pp. 1186-1190.

[4] H.-J. Lee, D. S. Ha, and H.-S. Lee, "A frequency-domain approach for all-digital CMOS ultra wideband receivers," *IEEE Conference on Ultra Wideband Systems and Technologies*, Reston, VA, Digest of Papers, November 2003.

[5] C. Schiller and P. Byrne, "An 4 GHz 8b ADC system," *IEEE Journal on Solid-State Circuits*, vol. 26, pp. 1781-1789, Dec. 1991.

[6] M. McTigue and P. J. Byrne, "An 8-gigasample-per-second 8-bit data acquisition system for a sampling digital oscilloscope," *Hewlett-Packard Journal*, pp. 11-13, 1993.

[7] C. R. Anderson, A. M. Orndorff, R. M. Buehrer, and J. H. Reed, "An Introduction and Overview of Ultra Wideband Communications," MPRG Technical Report, Virginia Polytechnic Institute and State University, May 2004.

[8] N. Kurosawa, H. Kobayashi, K. Maruyama, H. Sugawara, and K. Kobayashi, "Explicit analysis of channel mismatch effects in time-interleaved ADC systems," *IEEE Transactions on Circuits and Systems I*, vol. 48, No. 3, pp. 261-271, March 2001.

[9] —, "±5V, 1Gsps, 8-Bit ADC with on-chip 2.2 GHz track/hold amplifier," Product Datasheet, Maxim Integrated Products, 2002.

[10] C. R. Anderson, "A software defined ultra wideband transceiver for communications, ranging, or imaging," Ph.D. Dissertation, Virginia Polytechnic Institute and State University, December 2006.

[11] W. C. Black, Jr, "High speed CMOS A/D conversion techniques," Ph.D. Dissertation, University of California, Berkeley, December 1980.

[12] A. M. Orndorff, "Transceiver design for ultra wideband communications," Masters Thesis, Virginia Polytechnic Institute and State University, http://scholar.lib.vt.edu/theses/index.html, May 2004.

[13] L. Yang and G. B. Giannakis, "Optimal pilot waveform assisted modulation for ultra-wideband communications," *IEEE Transactions on Wireless Communications*, vol. 3, no. 4, pp. 1236-1249, July 2004.

[14] C. R. Anderson, A. Annamalai, A. M. Attiya, N. August, R. M. Buehrer, W. A. Davis, M. X. Gong, S. Griggs, D. Ha, S. Licul, S. F. Midkiff, S. Muthuswamy, J. A. Neel, J. H. Reed, S. Riad, B. M. Sadler, A. Safaai-Jazi, D. G. Sweeney, W. Tranter, *An Introduction to Ultra Wideband Communications*, New Jersey: Prentice Hall, 2005.

Performance analysis of a time-interleaved sampling architecture for a software defined ultra wideband receiver

MPRG

MOBILE & PORTABLE RADIO RESEARCH GROUP

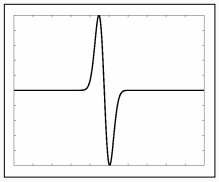
Christopher R. Anderson

Jeffrey H. Reed

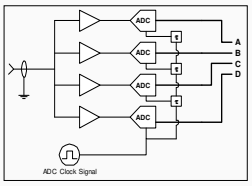
November 14, 2005

Virginia Tech

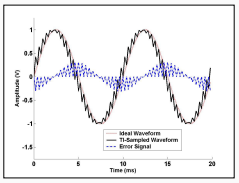
Presentation Overview



Overview of UWB Signals



UWB SDR Architecture:
Time Interleaved Sampling



TI-Sampling of UWB Pulses:
Simulated Performance Results

MPRG

MOBILE & PORTABLE RADIO RESEARCH GROUP

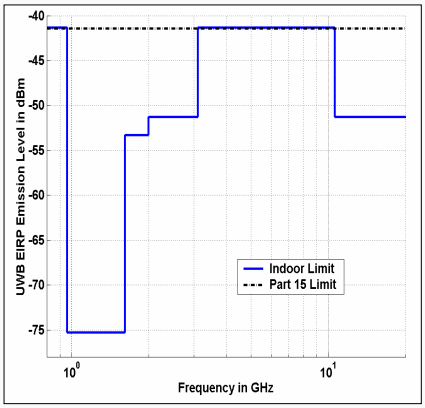
A brief overview of UWB signal characteristics

The FCC allows unlicensed UWB signals which meet a specific spectral mask.

The predicted use for UWB communication is short-range, high-data rate communications.

Note: Although impulse-based modulation is assumed by many, it is not required by the FCC.

Note: Energy transmitted by UWB systems will add to the noise floor of existing users.



Power Level: - 41 dBm/MHz
Frequency: 0 – 960 MHz
3.1 – 10.6 GHz

MPRG
MOBILE & PORTABLE RADIO RESEARCH GROUP

The Impulse UWB (I-UWB) pulse shape

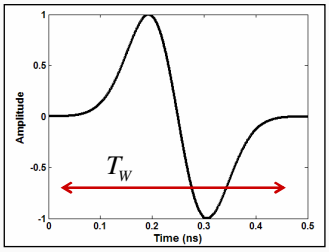
UWB Pulses are typically modeled as Gaussian Pulses or Gaussian Monocycles with durations ranging from 100ps – 1 ns.

$$p(t) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(t-\mu)^2}{2\sigma^2}}$$

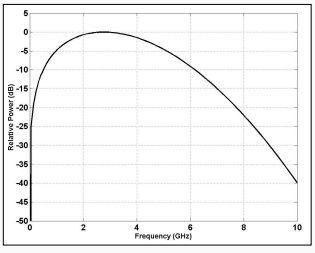
$$p'(t) = \frac{(t-\mu)}{\sigma^2} e^{-\frac{(t-\mu)^2}{2\sigma^2}}$$

$$\sigma = \frac{T_W}{2\pi}$$

Note: Pulses are normalized to unit amplitude

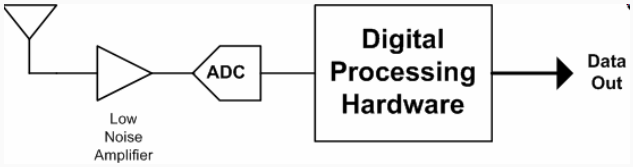


Gaussian Monocycle & Its Spectrum



MPRG
MOBILE & PORTABLE RADIO RESEARCH GROUP

Problems associated with SDR for Ultra Wideband.



Problem:

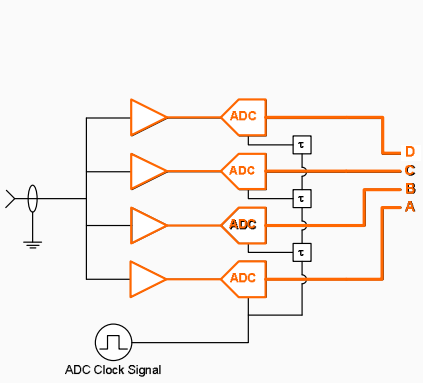
To digitize a 500 ps UWB pulse requires a sampling rate of 8 GS/s.
At 8 bits/sample, receiver must process 64 Gbps in real time!

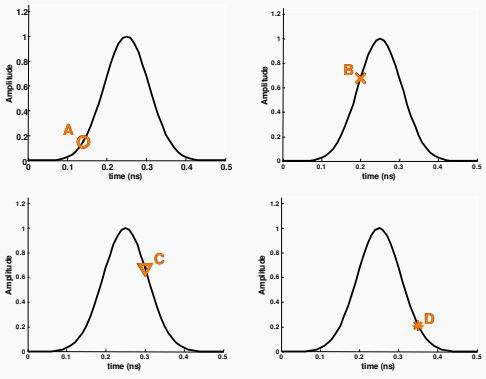
Current Solutions

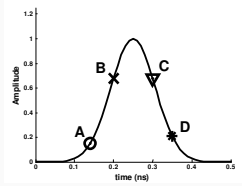
Equivalent Time Sampling
Frequency Domain Sampling
Time-Interleaved Sampling

MPRG
MOBILE & PORTABLE RADIO RESEARCH GROUP

Receiver Architecture – Time Interleaved (TI) Sampling

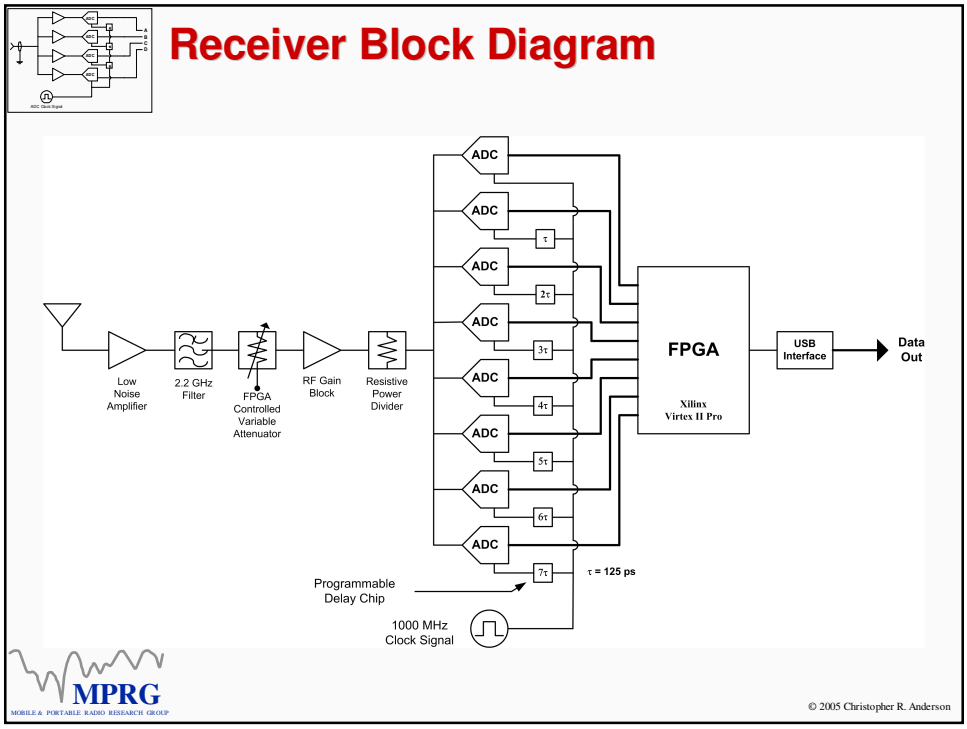


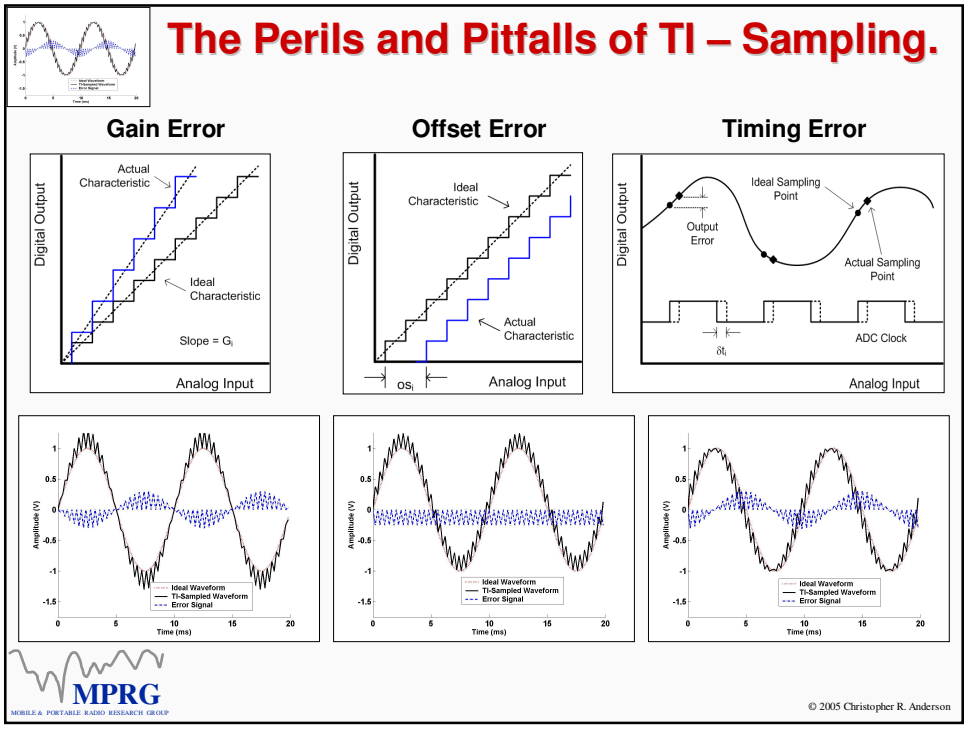


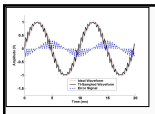


MPRG
MOBILE & PORTABLE RADIO RESEARCH GROUP

Christopher R. Anderson



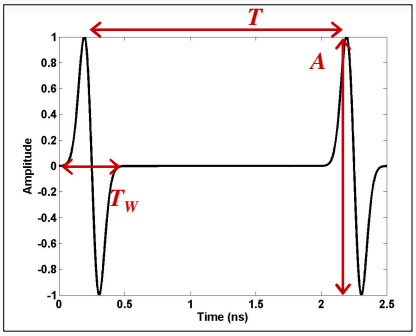




TI-Sampling a Gaussian Monocycle: Important Terminology.

Simulation Parameters

- 3 Different Pulse Widths
- T = 10 ns (100 MHz prf)
- 8 ADCs / 8 GHz Sampling Frequency
- Target of 6 dB Reduction in $SNR_{Effective}$
- Results averaged over 25,000 trials



SNR due to TI-Sampling Mismatches

$$SNR_{Effective} = SQNR_{Ideal} - SNR_{Mismatch}$$

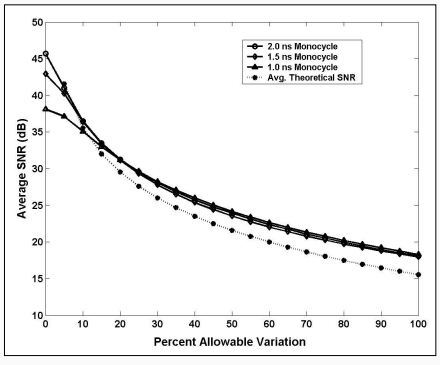
$$SQNR_{Ideal} = 8.59 + 6.02B + 10\log_{10}\left(\frac{T_W}{2\pi T}\right) \quad [dB]$$

$$SNR_{Mismatch} = 10\log_{10}\left(\frac{\sum_{i=0}^{N-1} x_i^2}{\sum_{i=0}^{N-1}(x_i - y_i)^2}\right) \quad [dB]$$

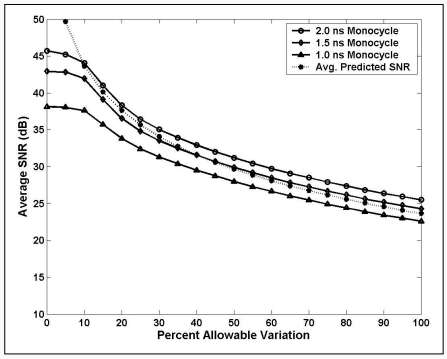
MPRG
MOBILE & PORTABLE RADIO RESEARCH GROUP

TI-Sampling a Gaussian Monocycle: Gain and Offset Mismatch.

Gain Error



Offset Error



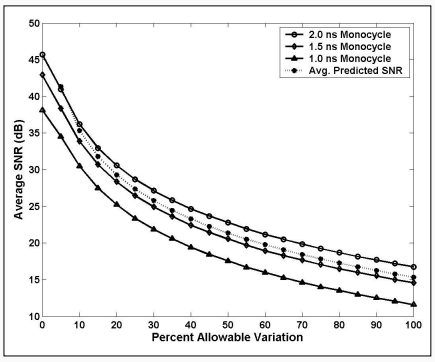
100% Variation equals ±50% Gain
6 dB Reduction in $SNR_{Effective}$ at ±5%

100% Variation equals ±5.5 LSBs
6 dB Reduction in $SNR_{Effective}$ at ±20%

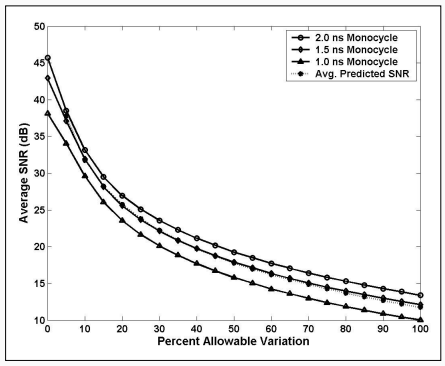
MPRG
MOBILE & PORTABLE RADIO RESEARCH GROUP

TI-Sampling a Gaussian Monocycle: Timing and Total Combined Mismatch.

Timing Error



Total Combined Error

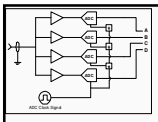


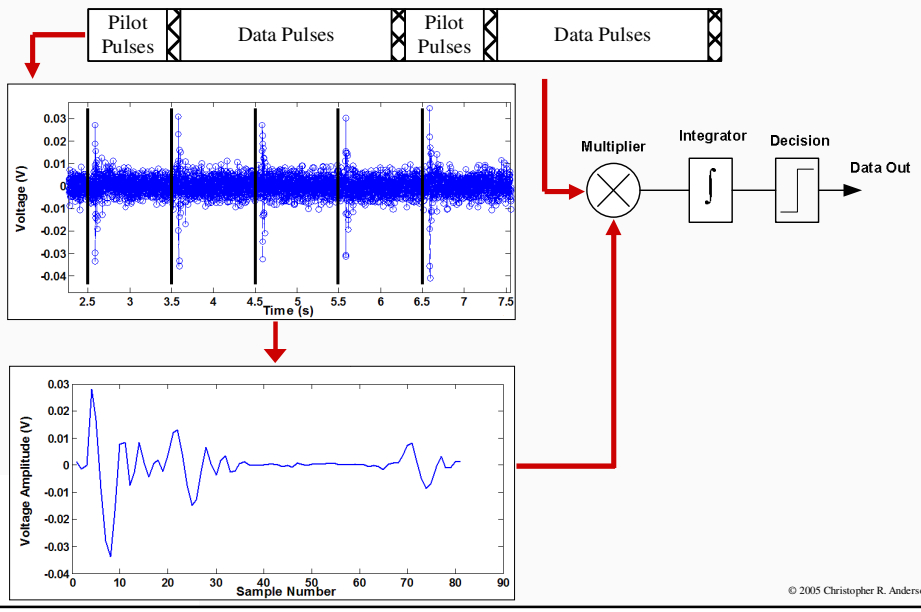
100% Variation equals ±125 ps
6 dB Reduction in $SNR_{Effective}$ at ±7%

100% Variation equals:
±5.5 LSBs / ±50% Gain / ±125ps
6 dB Reduction in $SNR_{Effective}$ at ±5%

MPRG
MOBILE & PORTABLE RADIO RESEARCH GROUP

Pilot Based Matched Filter Receiver can compensate for static mismatches.



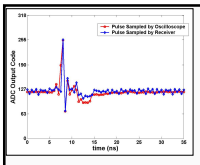


Acknowledgements

Funding Sources: Office of Naval Research (Primary Sponsor), ASPIRES, Bradley Fellowship, Virginia Space Grant Fellowship

Significant Contributors

XILINX, molex, DRS TECHNOLOGIES, CPES, Mentor Graphics, freescale semiconductor, DRT Digital Receiver Technology, Inc., LINEAR TECHNOLOGY, ANDREW, NOVA ENGINEERING, ON Semiconductor, signal consulting inc, MPRG MOBILE & PORTABLE RADIO RESEARCH GROUP, DALLAS SEMICONDUCTOR, MAXIM



Conclusions

The UWB SDR is designed to be an extremely flexible Testbed for Impulse UWB signals.

The SDR Testbed also could conceivably be reconfigured to operate with most broadband signals.

TI-Sampling UWB pulses is feasible, but ADC mismatches must be very carefully controlled.

Questions?

MPRG MOBILE & PORTABLE RADIO RESEARCH GROUP