Sample Rate Converter for Digital Modulator

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Why SDR needs SRC

- Many standards: many symbol/ship Rates
- SDR prefers common DAC/ADC clock source
- Example: GSM/EDGE/WCDMA Modulator
  - **270.833 ksym/s (GSM/EDGE)**
  - **3.84 Msym/s (WCDMA)**

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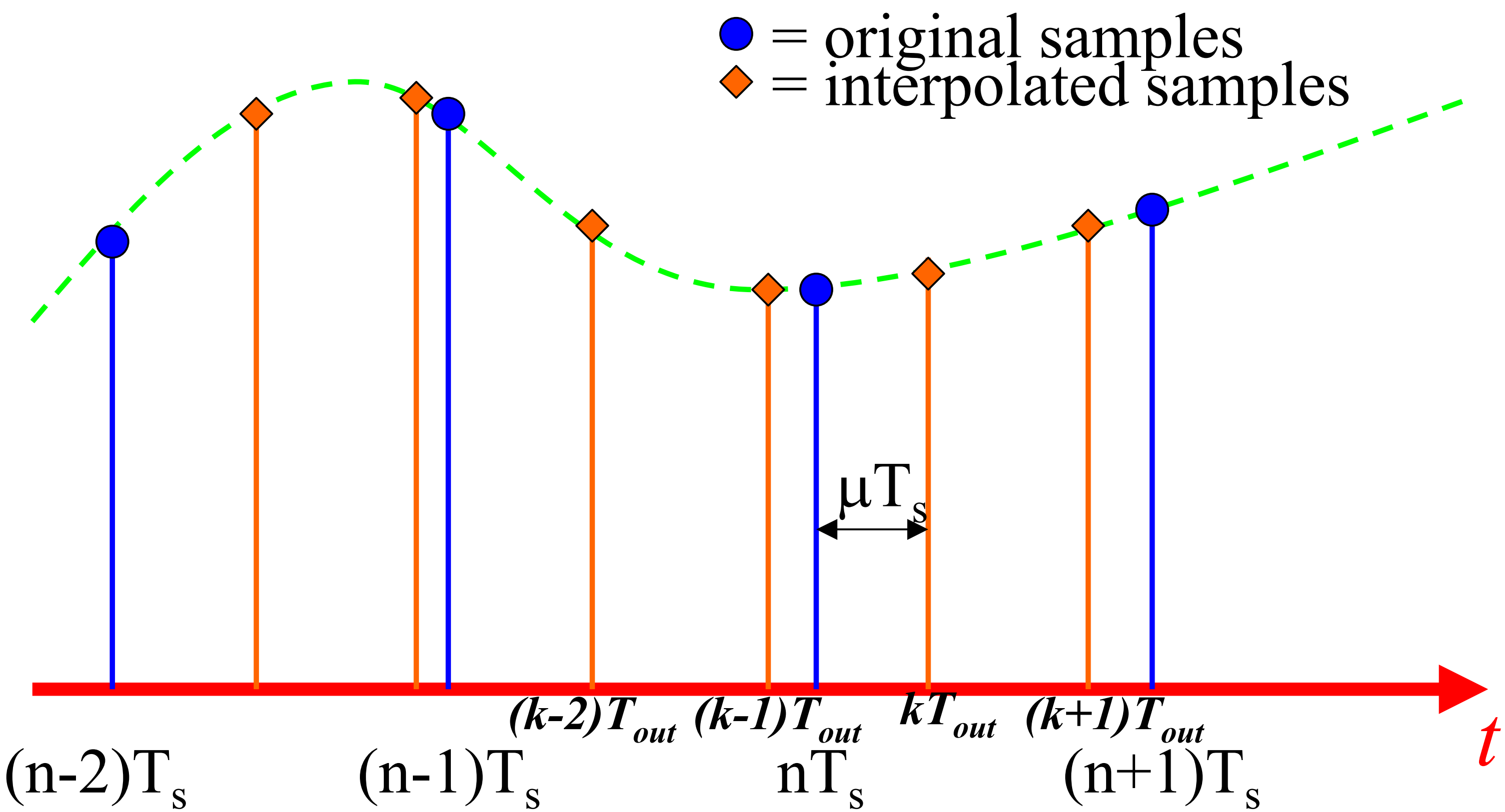
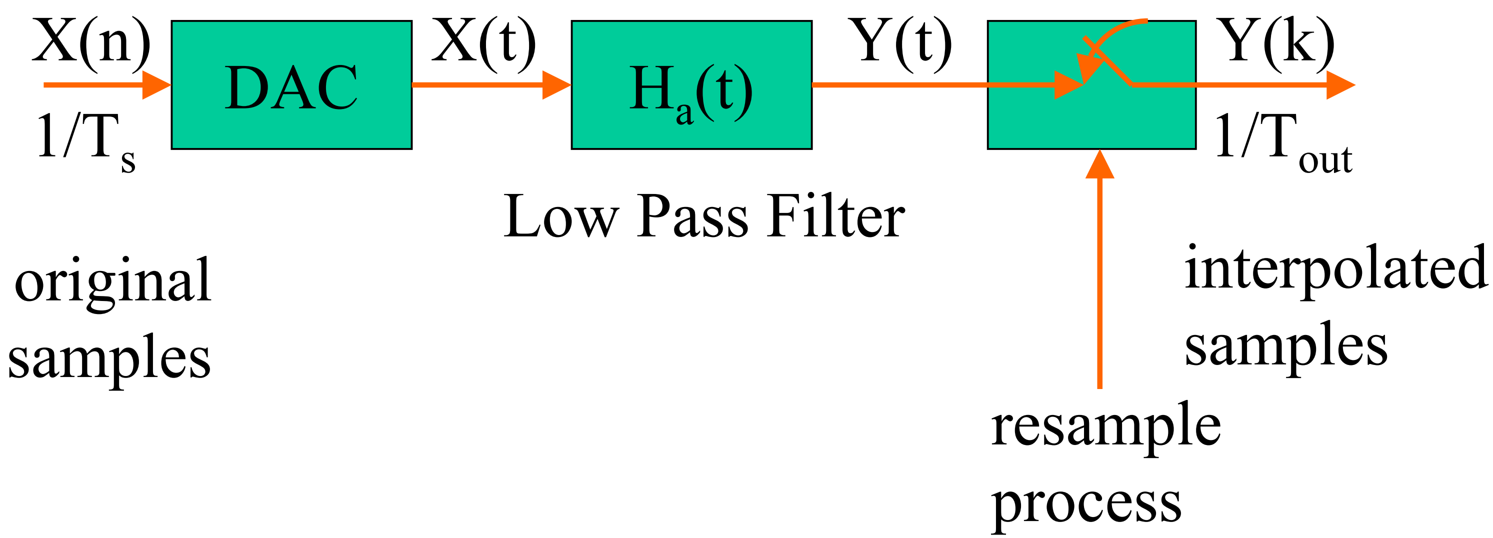
Time-domain Interpolation

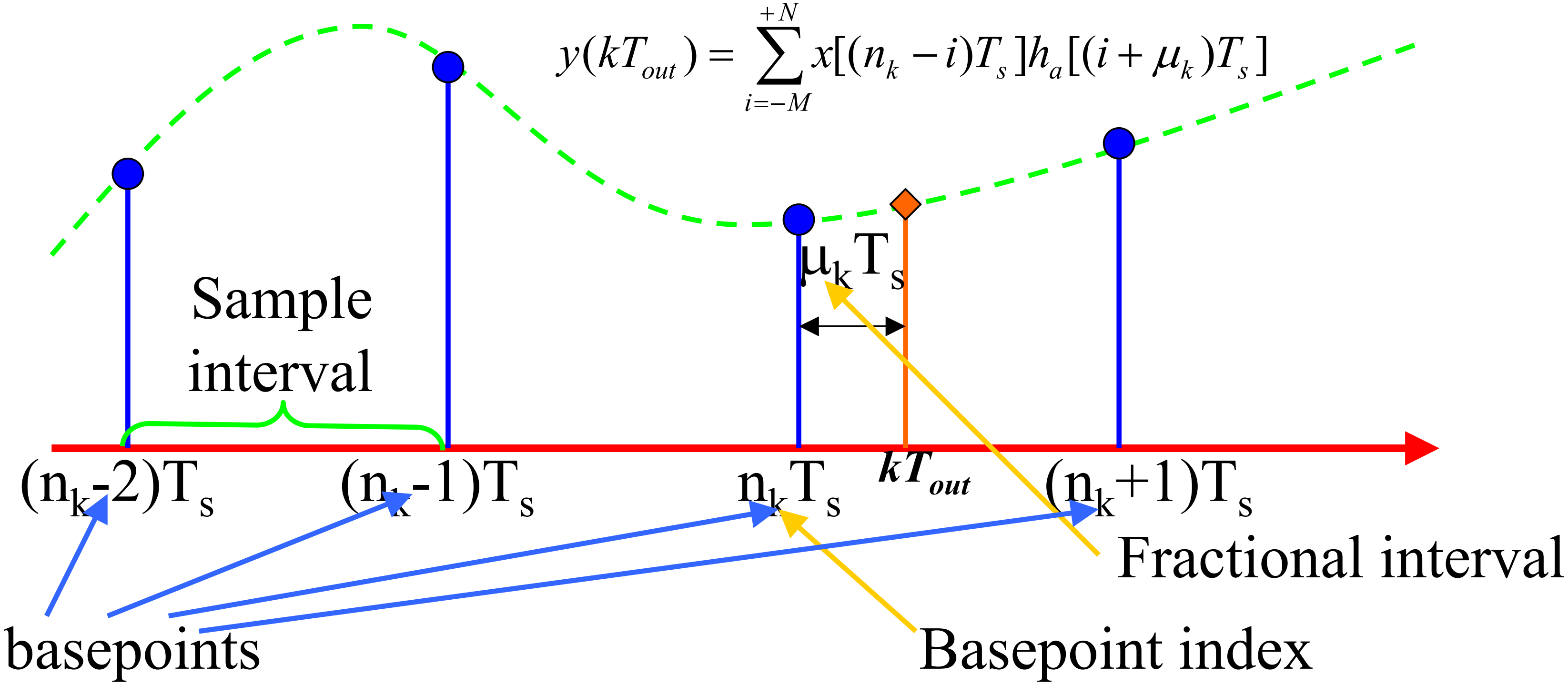


A Hybrid Analysis Model



All Digital SRC

$$y(kT_{out}) = \sum_{i=-M}^{+N} x[(n_k - i)T_s]h_a[(i + \mu_k)T_s]$$



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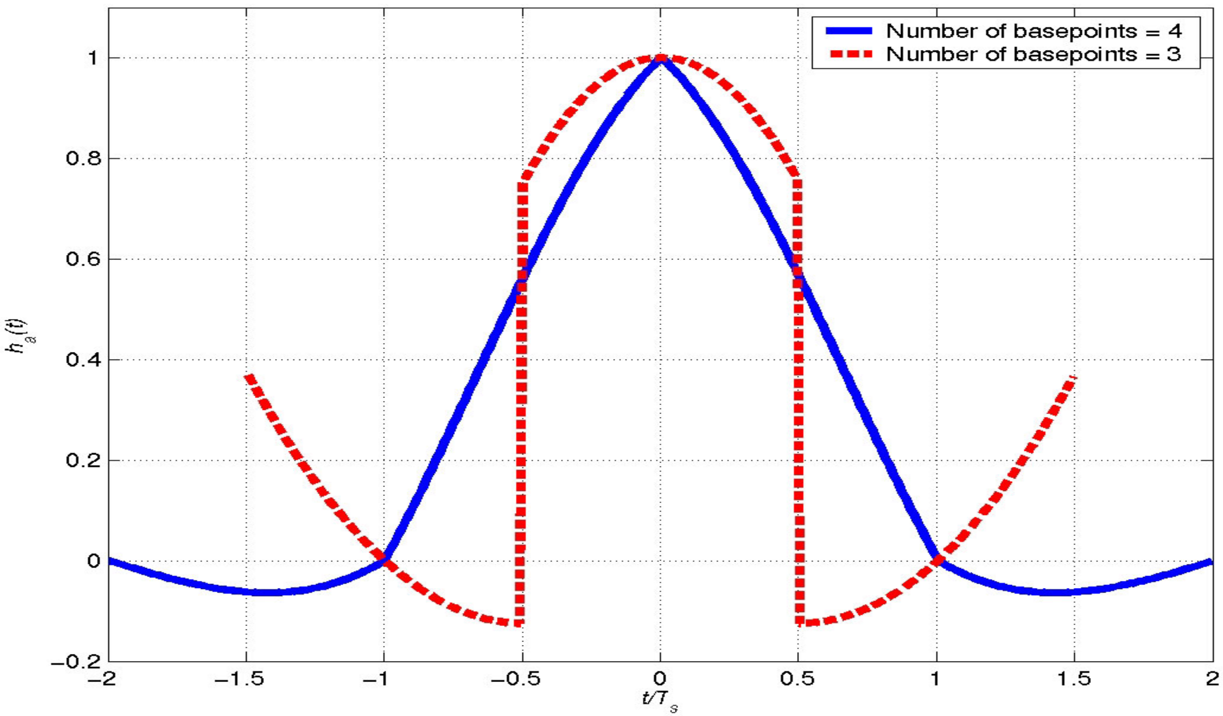
Traditional FIR Implementation

- Each output is an FIR operation
- FIR coefficients vary with fractional interval μ_k
- Large memory requirements when $\{\mu_k\}$ gets large:
  - **4 basepoints**
  - **μ_k: 8 bits representation**
  - **Coefficients: 16 bits representation**
  - **ROM size: $4*16*2^8 = 16384$ bits**

Why Polynomial Based SRC

- Filter response is piecewise polynomial of μ_k in each sample interval
- Coefficients can be calculated on line based on μ_k
- Hardware efficient implementation structure: Farrow structure
- Example: Lagrange polynomial based SRC

Impulse Response of Linear Phase Lagrange Polynomial Based SRC



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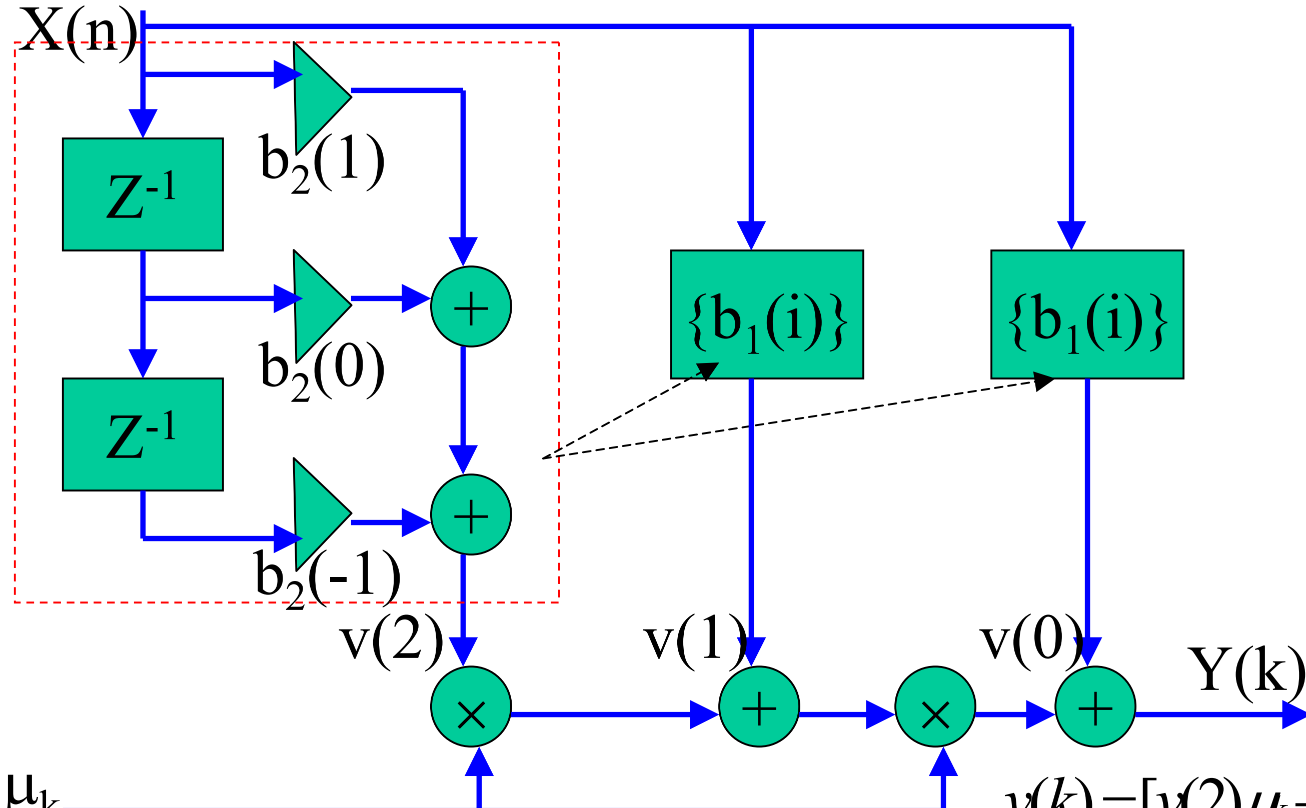
Farrow Structure: Nested Polynomial Evaluation

$$y(k) = \sum_{i=-M_1}^{M_2} x(n-i) \sum_{l=0}^{N-1} b_l(i)(\mu_k)^l$$

$$= \sum_{l=0}^{N-1} (\mu_k)^l \sum_{i=-M_1}^{M_2} b_l(i) x(n-i)$$

$$= \sum_{l=0}^{N-1} (\mu_k)^l v(l), v(l) = \sum_{i=-M_1}^{M_2} b_l(i) x(n-i)$$

Farrow Structure: Implementation

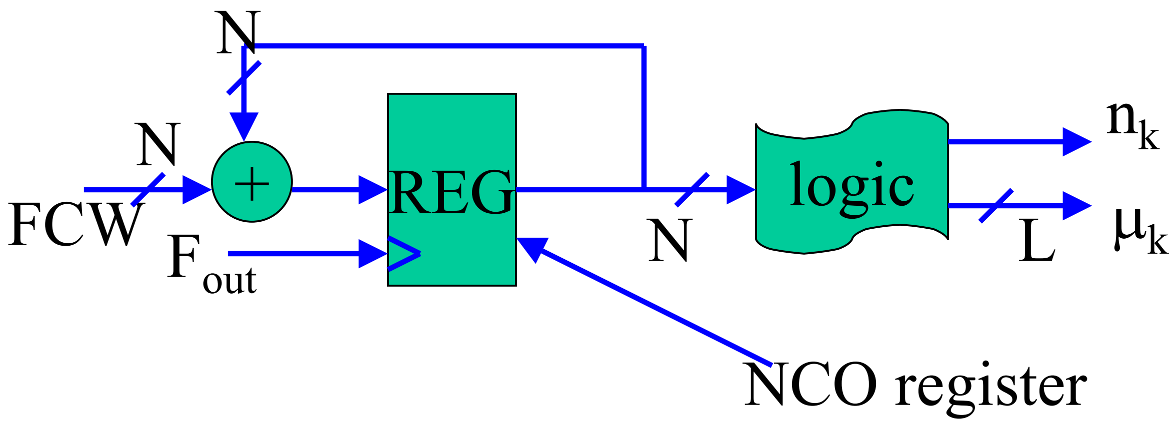


$$y(k) = [v(2)\mu_k + v(1)]\mu_k + v(0)$$

SRC Implementation: Key Pieces

- The basepoint index n_k
- The fractional interval μk
- The Farrow structure for computation

Numerically Controlled Oscillator: SRC Control



- FCW = F_{in}/F_{out} ($F_{in} < F_{out}$)
- NCO register overflows at the rate of F_{in}
- N determines the frequency resolution

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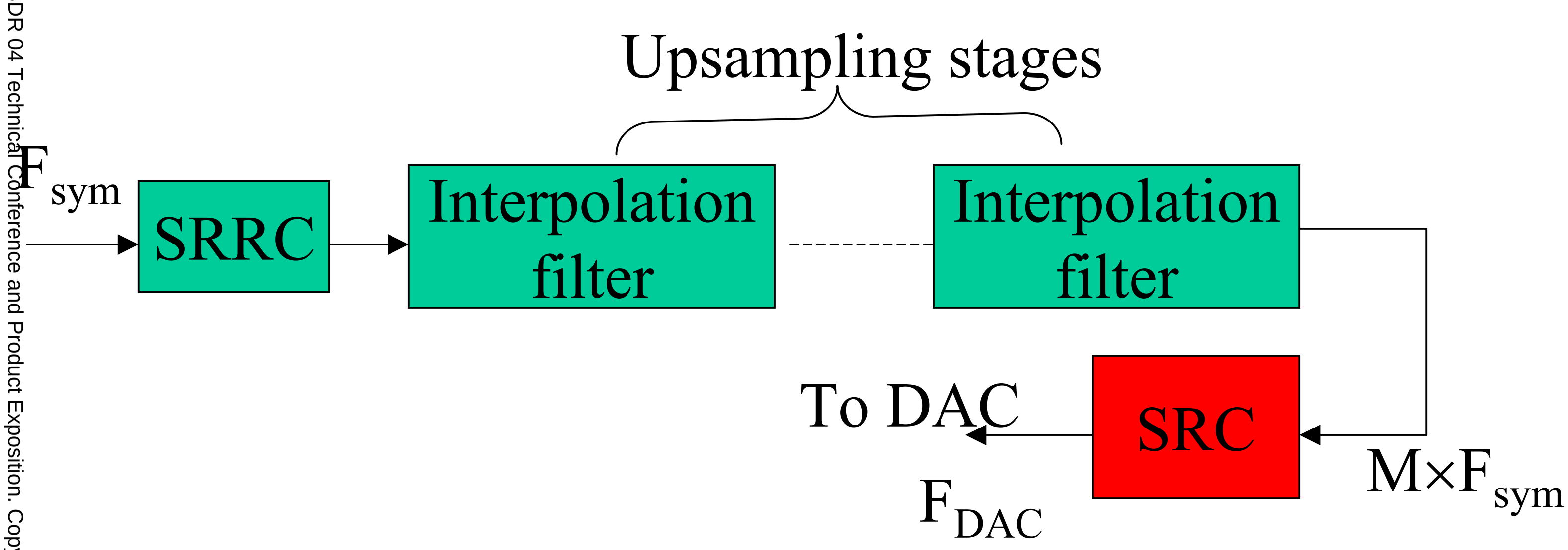
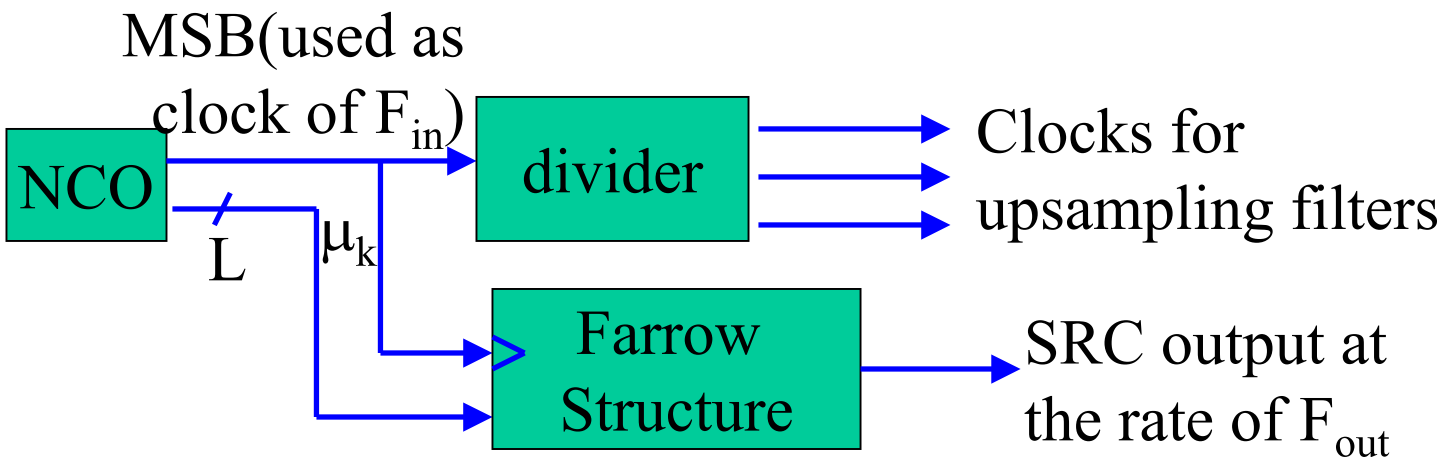
Digital Modulator Architecture



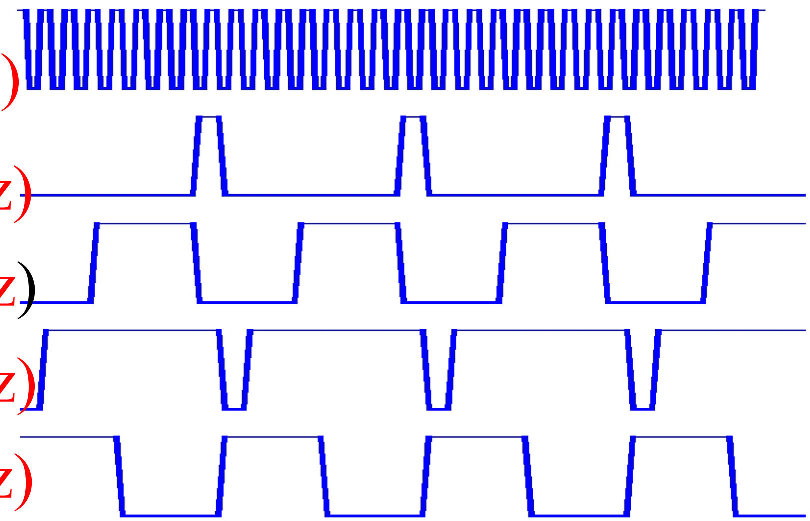
- Arbitrary F_{DAC} not related to F_{sym}

Techniques Used in References



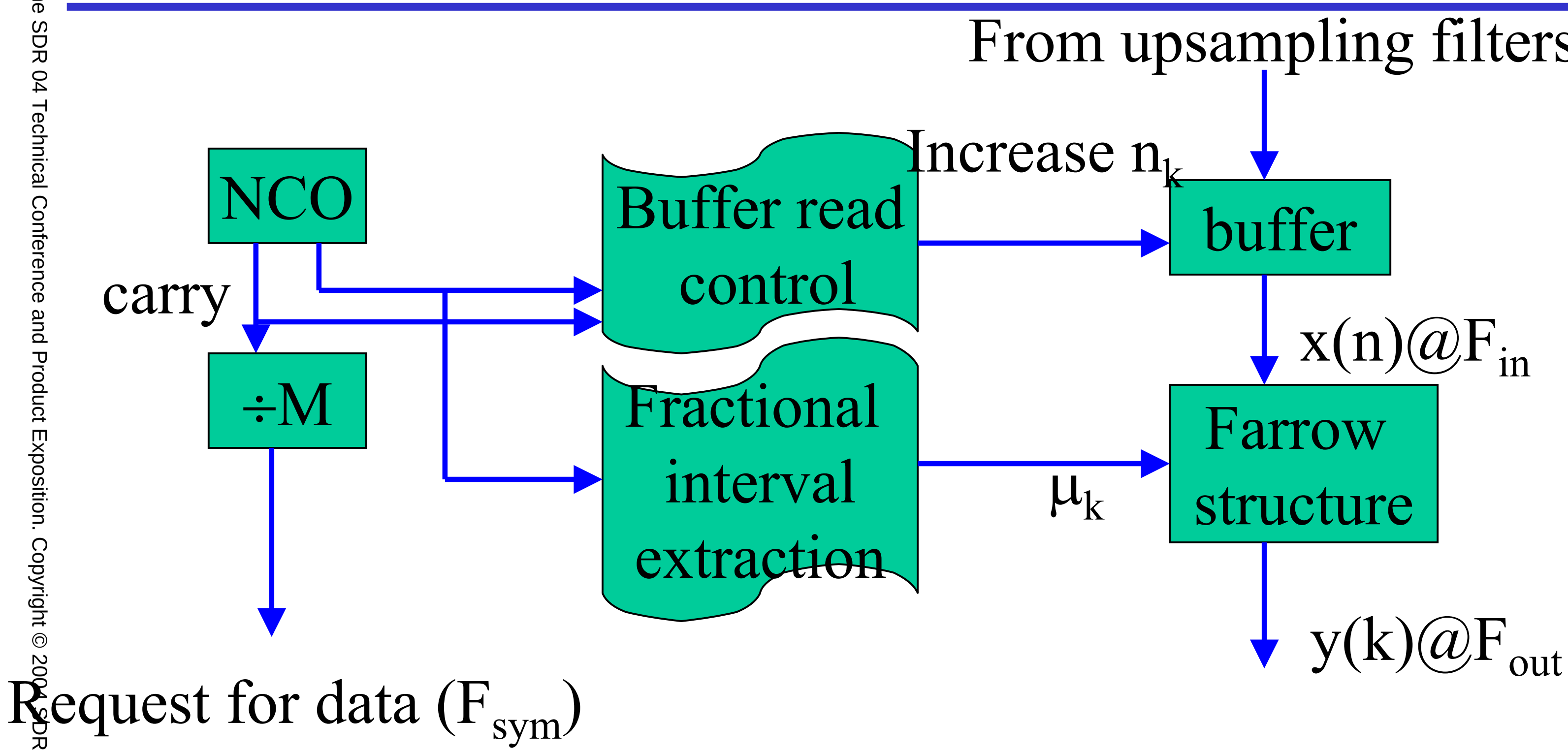
- F_{out} needs to be at least twice higher than F_{in}
- Different clocks for different stages of upsampling filters: difficult for software implementation

Why $F_{out} \geq 2F_{in}$



- MSB is assumed to toggle when NCO overflows

New SRC Architecture



Why the Buffer

- Decouples the upsampling filter from output clock rate
- Allows upsampling filters to be implemented using software
- “request for data” signal guarantees the balance of the buffer

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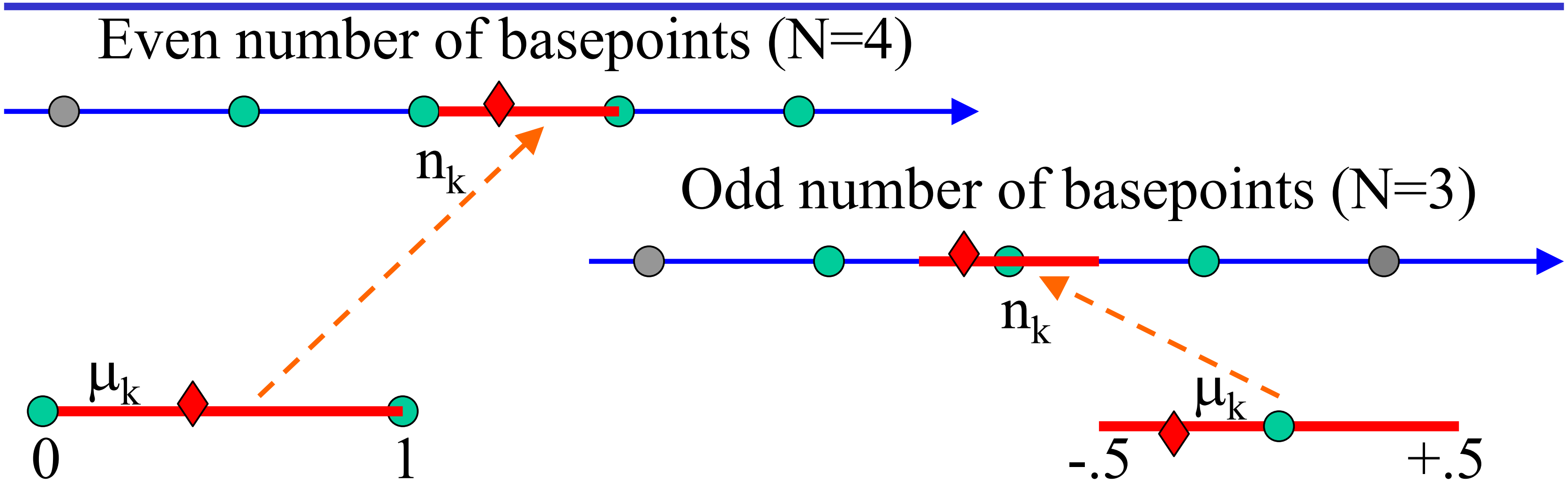
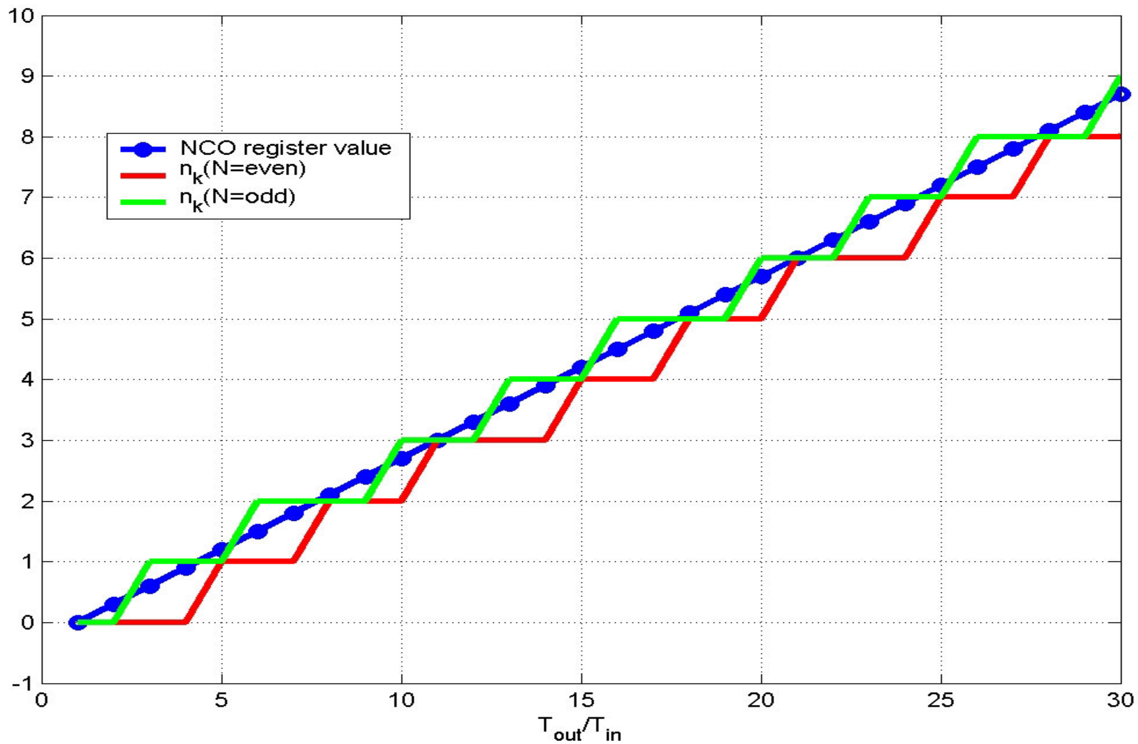
Basepoint Index n_k and Fractional Interval μ_k



- Perform interpolation in the center interval
- Guarantee linear phase property of the interpolation filter

n_k vs. NCO



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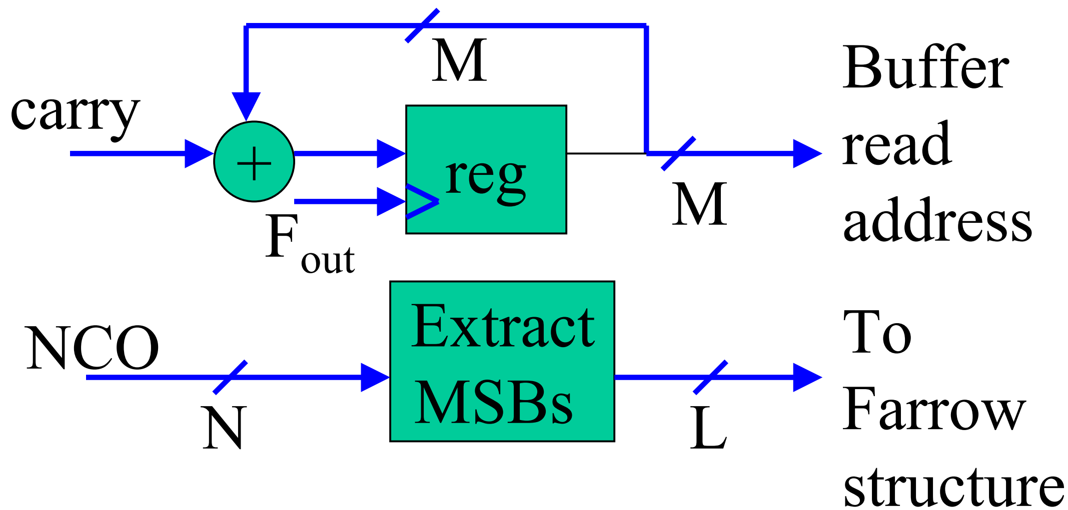
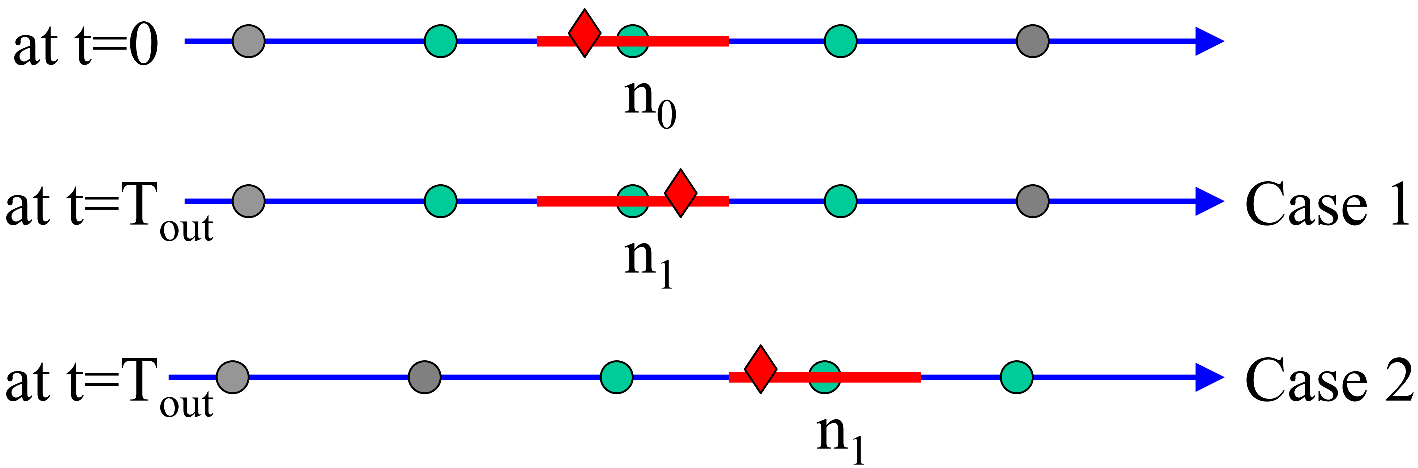
SRC Control for Even Number of Basepoints



Odd Number of Basepoints: Whether to Increment n_k



- Depends on these factors
  - **Previous NCO register value ≥ 0.5 ?**
  - **Current NCO register value overflows?**
  - **Current NCO register value ≥ 0.5 ?**

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Control Logic for n_k Increment

Case #	$NCO_{k-1} \geq 0.5$	$carry_k$	$NCO_k \geq 0.5$	Increase n_k
1	Y	1	N	0
2	Y	1	Y	1
3	Y	0	Y	0
4	N	1	N	1
5	N	0	Y	1
6	N	0	N	1

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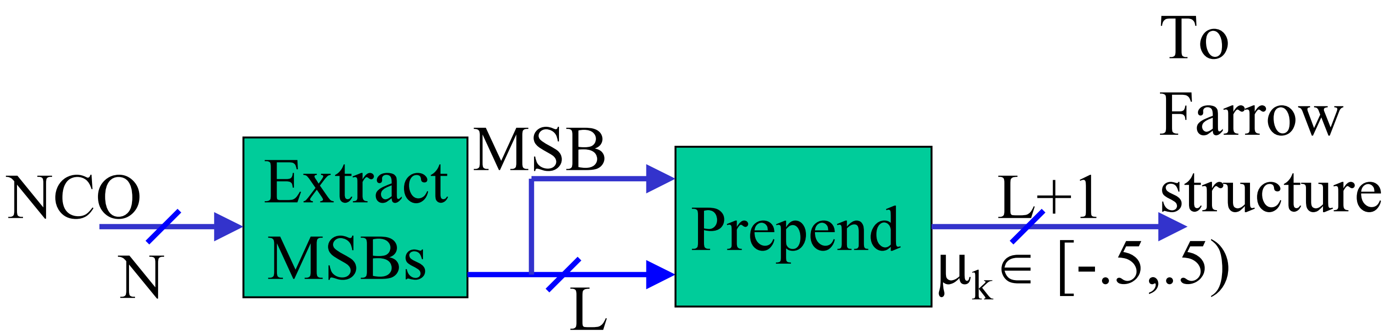
Fractional Interval Extraction (N = Odd)



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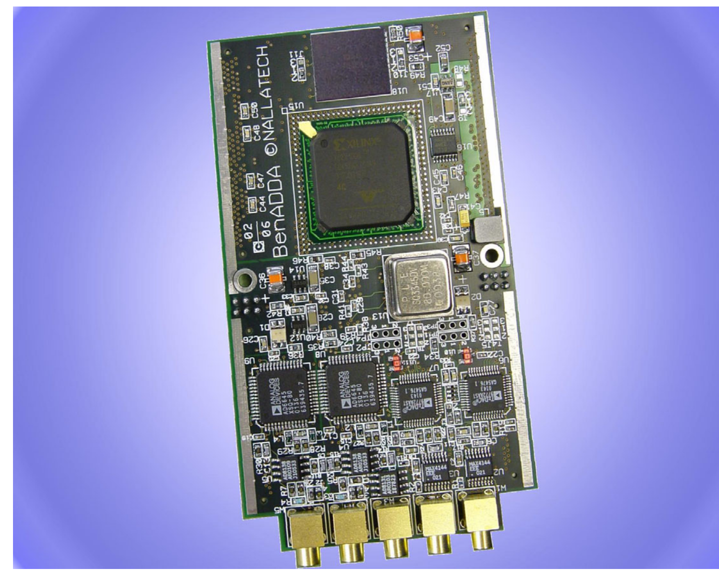
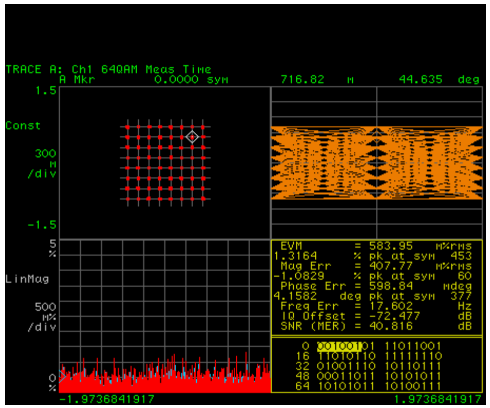
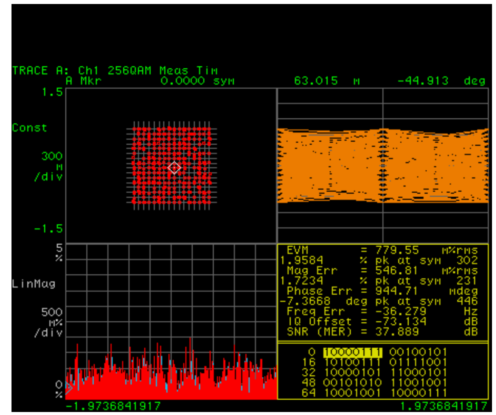
A Digital Modulator Example

- Digital video broadcasting system (ITU J.83 Annex B standard)
- 64QAM: ~5.057 Msym/s
- 256QAM: ~5.36 Msym/s
- DAC clock = 100 MHz



Dual Channel Modulator Performance





- Two channels: 64QAM + 256QAM
- Polynomial based SRC (3 basepoints) after 16x interpolation
- EVM < 1%, ACPR > 65dB

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Summary

- Sample Rate Converter (SRC) for digital modulator
- Polynomial based SRC and Farrow structure
- SRC architecture and implementation
- Digital modulator design demonstration and satisfactory performance