CHANNELIZATION TECHNIQUES FOR SOFTWARE DEFINED RADIO

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ABSTRACT

The ability to support multiple communications channels per RF band is a fundamental process for many software defined radio platforms. These platforms typically employ a channelizer to extract channels from the received RF band for follow-on baseband processing, or to insert channels into the RF band for transmission. This paper will compare and contrast three of the more popular channelization techniques: Digital Down Conversion, Frequency Domain Filtering, and Polyphase FFT Filter Banks. The analysis begins by presenting a base architecture for a wideband transceiver, and then explores each channelization method within the context of this architecture. These include the computational complexity of the channelization approach, the applicability of the approach in supporting a given frequency plan, and processor selection for the proposed implementation.

1. INTRODUCTION

Wireless transceiver technologies typically break into either narrowband or wideband architectures, with narrowband systems typically supporting only a single carrier per RF channel and wideband systems supporting multiple simultaneous carriers. Narrowband architectures are often utilized in portable radios, including cellular handsets and tactical communications systems, where support for multiple channels is typically not necessary, and the interference rejection inherent in the narrowband architecture is important (see Figure 1). Conversely, wideband architectures are often utilized for infrastructure systems, including cellular base stations, tactical communications gateways, and satellite communications hubs, where dozens or even hundreds of simultaneous carrier channels may be active at any one time. Wideband architectures are also useful in a number of niche applications for military and civil defense, including signals intelligence and electronic warfare.

A key element of the wideband receiver architecture is the channelization technique that is used to isolate the independent communication channels contained within the wideband signal. This paper will explore several of the predominant channelization techniques utilized in wideband transceiver systems, including examining some of the practical aspects of implementation of each channelization method in a software defined radio platform. The paper will focus primarily on receiver architectures, but the techniques and analysis presented are equally applicable for transmission as well.

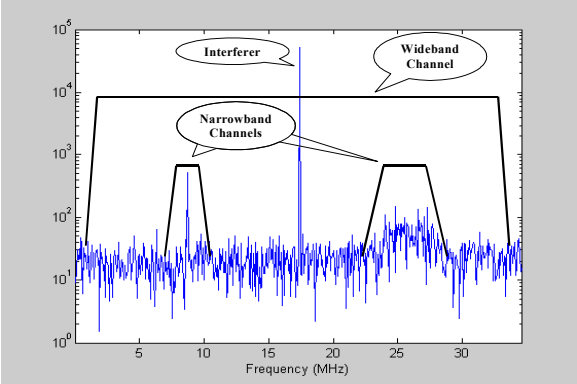

Figure 1: Wideband and Narrowband Channels

2. BASE ARCHITECTURE OF A CHANNELIZED TRANSCEIVER

The base architecture for a wideband transceiver is presented in Figure 2 [1]. In this architecture, a single channelization engine supports multiple channel processing elements. On the receive side, the channelizer extracts the channels of interest from the digitized RF bands, and then forwards these channels on to channel processing for demodulation and decoding. This process is reversed on the transmit side, with payload data encoded and modulated in the channel processors and then inserted into the output signal by the channelizer for retransmission. The number of channel processors supported by the channelizer is set based on the target number of active carriers operating at any given time.

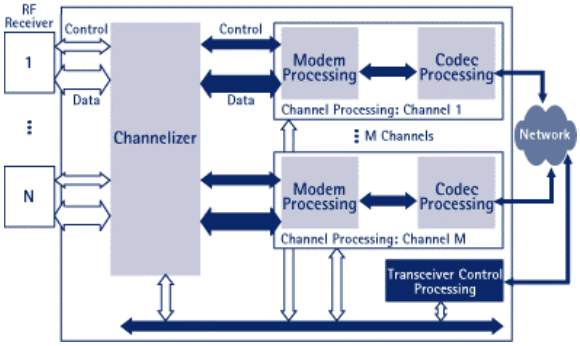

Figure 2: Typical Architecture for Wideband Transceiver

The interface between the channelizer and the RF front end in this architecture comes from the analog conversion subsystem within the digital transceiver. Two

conversion techniques are typically employed: IF sampling and Zero-IF conversion (see Figure 3). In IF sampling systems the wideband channel into and out of the transceiver is centered at a predefined intermediate frequency (IF). In a Zero-IF conversion scheme, the wideband signal is converted to baseband with inphase (I) and quadrature (Q) channels passed between the RF front end and the converter devices.

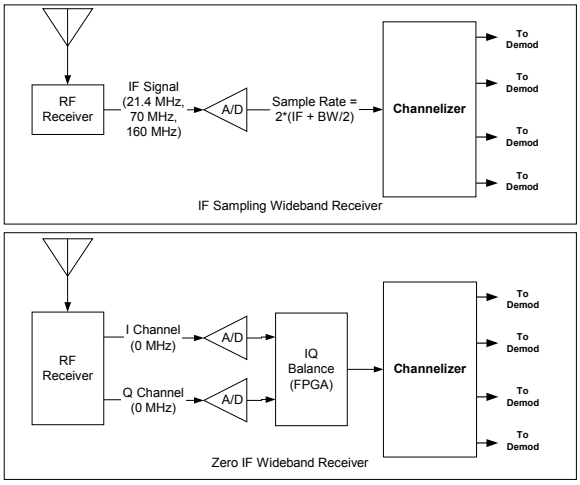

Figure 3: Front End Architectures for Wideband Receivers

IF Sampling typically requires front end channelization processing to operate at a significantly higher rate than a Zero-IF scheme for a given bandwidth. For example, a 70 MHz IF signal with 60 MHz of bandwidth requires a sampling rate of greater than 200 MSPS. This same bandwidth can be supported through baseband sampling at 60 MSPS, allowing the channelization processing engine to operate at a much lower rate. Note that, in general, dynamic range decreases as sample rate increases, so identifying a converter device with sufficient dynamic range for a target application may be problematic in an IF Sampling architecture.

The Zero-IF technique also comes at a price: in a Zero-IF architecture an imbalance in the amplitude or phase of the I and Q arms of as little as a tenth of a dB can reduce the available dynamic range to less than 40 dB [2]. Maintaining this level of balance prior to the A/D converters is problematic, and as such compensation for IQ imbalances must occur in the digital domain prior to channelization processing. A number of techniques are available to support IQ balancing, some of which may be incorporated directly into the channelizer engine, depending on the channelization approach [3, 4, 5].

3. ISSUES DRIVING THE CHANNELIZATION ARCHITECTURE

Two key issues defining the technical requirements of the channelizer are the spectral content of the wideband channel of interest and the types of processing devices available for channelization processing. These issues are discussed in detail in the following sections.

3.1. Spectral Content of the Wideband Channel

The technical requirements for the channelization approach chosen are driven by the frequency allocation plans supported by the software defined radio. At one extreme is cellular communications, where the system architecture typically defines a fixed carrier spacing with a constant RF bandwidth per carrier channel. For example, GSM900 defines an uplink band from 890 to 915 MHz and a downlink band from 935 to 960 MHz (see Figure 4) [6]. Both of these bands contain 124 carrier channels spaced 200 kHz apart. The channelizer supporting this type of network may be able to utilize the redundancy of the channel structure to provide an efficient channelization mechanism.

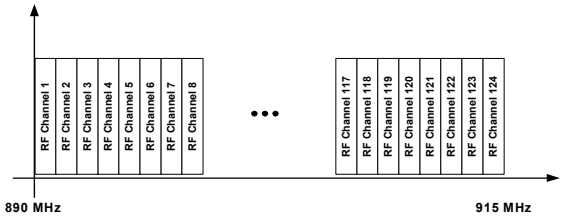

Figure 4: Uplink RF Channel Structure for GSM900

At the other extreme, both the carrier frequency and RF bandwidth per carrier are dynamically assigned. This type of architecture is found in a multi-standard communications system such as a multi-standard satellite gateway [7, 8, 9]. In these types of systems, subscribers may be assigned a waveform specific to a service offering, or may be assigned an operating mode for a waveform based on pre-defined requirements for quality of service. The carrier frequency, synchronization scheme, and analog bandwidth parameters of each subscriber signal will vary depending upon the specified operating parameters of the assigned waveform (see Figure 5). The channelizer employed in a radio supporting this type of architecture must be flexible enough to accommodate all of the carrier/bandwidth combinations supported by the network architecture, and possibly allow for the dynamic reallocation of channel resources within this architecture during operation [10].

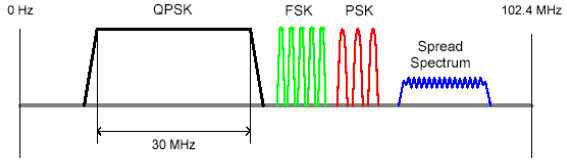

Figure 5: Possible Frequency Plan for Wideband Satellite Radio Link [11]

3.2. Processor Selection for Channelization Processing

In an ideal software defined radio architecture, processing would be limited to general purpose processors (GPPs) communicating with standards based protocols, such as TCP/IP or CORBA. This model allows for maximum reuse of application code across multiple platforms, accelerating time to market and maximizing the return on investment in application software through code reuse and upgradability [12]. In general, however, this type of operating environment is not practical in a field deployable system for two primary reasons:

- The power utilization and heat dissipation of GPPs are often prohibitive in many size, weight, and power limited systems. As a result, Digital Signal Processors (DSPs) are often utilized to supplement the processing provided by the GPP to keep the architecture within the specified power budget.

- GPPs and DSPs employ a serial processing architecture that does not provide sufficient performance for the processing of wideband signals. As such, the use of Field Programmable Gate Arrays (FPGAs), which gives near ASIC like performance in a programmable device, is often required in the SDR platform.

For these reasons, a heterogeneous processing engine incorporating a combination of FPGAs, DSPs, and GPPs is typically required in the digital transceiver architecture. Front-end channelization processing in this type of platform is typically limited to FPGAs due to performance constraints in dealing with the wideband input, although back-end processing which is preformed on a per channel basis may incorporate DSPs or GPPs.

4. CHANNELIZATION APPROACHES

The three predominant channelization architectures used in wideband communications systems are Digital Down Conversion (DDC), Frequency Domain Filtering, and Polyphase FFT Filter Banks. This section will explore each of these in detail.

4.1. Digital Down Conversion

A digital down converter provides the channelization function through a classic heterodyne technique [13]. In this technique, the wideband signal is mixed with a synthesized carrier at or near the carrier frequency of the channel of interest to baseband that channel. The resulting signal is then filtered and decimated to isolate and extract the channel of interest from the wideband signal and reduce the overall sample rate to the minimum necessary to support that channel (See Figure 6).

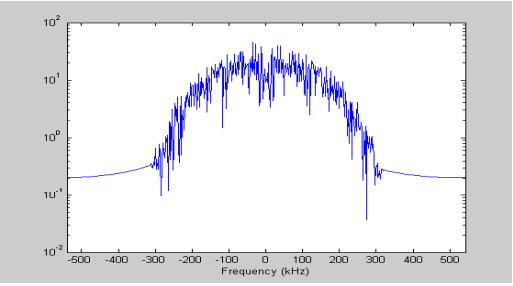

Figure 6:Baseband Channel Extracted from Wideband Signal Shown in Figure 1

Depending on the bandwidth of the channel of interest, one of two different filtering and decimation techniques are typically employed (See Figure 7). For wider bandwidth signals, requiring decimations of 8 or less, a wideband finite impulse response (FIR) filter is utilized directly following the baseband mixer. The output of this filter is then decimated by an appropriate amount. For narrower band signals, the filtering and decimation functions are typically split into multiple stages. The initial stage is provided by a Hogenauer filter, also known as a cascade integrator comb (CIC) filter, which provides for reasonable first stage channel isolation while minimizing the number of complex operations that must be performed prior to decimation [14]. Follow on filtering is typically then provided by a narrowband FIR filter, which would typically have programmable taps to allow this filtering to be optimized for the channel of interest.

The computational complexity of these algorithms is dependent upon the details of their implementation. At a minimum, the wideband DDC requires 6 operations for the mixing function and 6 operations per tap (2 multiplies, 2 adds, and 2 shifts) for the FIR filtering. The operations all occur prior to decimation at the input sample rate, and therefore the wideband DDC would most likely be implemented exclusively in an FPGA. Depending on the specific requirements, the wideband DDC could be implemented in less than a million gates in an FPGA, allowing up to six simultaneous wideband channels to co-exist in a large device such as an XC2V6000 [15].

Like the wideband DDC, the narrowband DDC also requires six operations for the mixing function. However, the pre-decimation filtering in this technique is limited to the cascade integrator portion of the CIC filter, requiring approximately six operations per stage. After decimation, the cascade comb portion of the CIC filter also requires six operations per stage, and six operations per tap are required for the FIR filtering. Since these latter operations occur at the decimated sample rate, the total operations per sample are significantly reduced over the equivalent wideband structure. As a result, up to three narrowband DDCs can occupy the same footprint as an equivalent wideband DDC, with an even higher number achievable if

the baseband processing is split between the FPGA and a DSP [15].

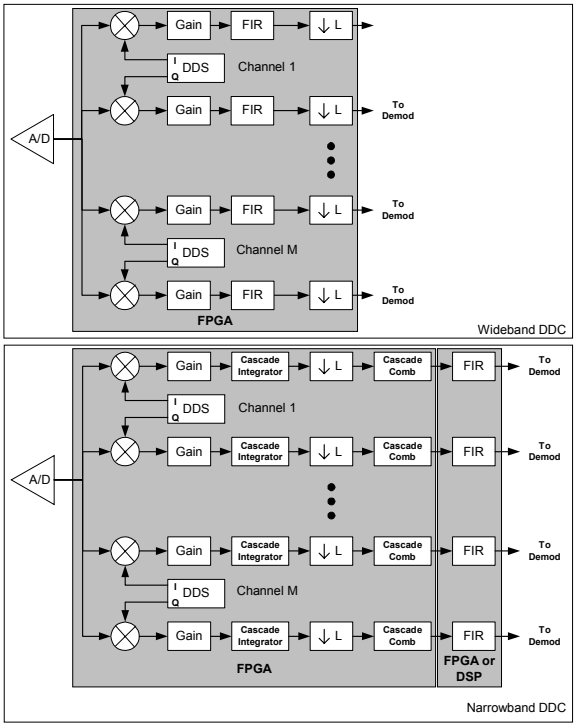

Figure 7: Channelization Architectures Using the Digital Down Conversion Approach

The primary advantages of the DDC techniques are the flexibility in selecting both the carrier frequency and channel bandwidth. However, for complex channel structures, where both wideband and narrowband channels may occupy the same input signal, a mix of down converter technologies may be required, complicating the architecture of the channelizer block.

4.2. Frequency Domain Filtering

The frequency domain filtering (FDF) approach makes use of the properties of the fast fourier transform (FFT) to simplify the baseband conversion, filtering, and decimation functions identified in the digital down converter approach [16, 17]. In this technique, input data is buffered into overlapping blocks, with an FFT performed on each of the blocks (see Figure 8). The FFT bins representing the frequency components for each channel of interest are extracted for follow-on processing, with the extraction process effectively performing the baseband mixing and decimation operations. Baseband filtering occurs by multiplying each bin in the resulting baseband signal by an associated filter coefficient representing the frequency response of the baseband filter using the "overlap-and-add" or "overlap-and-save" technique[18]. The resulting baseband signal is then reconverted to the time domain using an inverse FFT, with one inverse FFT performed for each carrier channel.

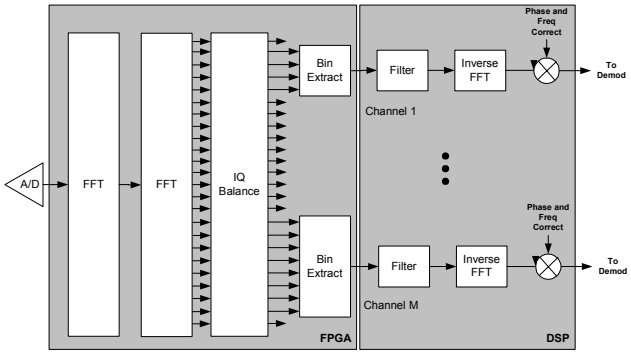

Figure 8: Channelization Architecture Using the Frequency Domain Filtering Approach

The computational complexity of the FDF Channelizer is driven by the initial FFT, requiring $NLog_xN$ operations, were N is the number of FFT bins and x is the FFT radix. For N equals 4096 points, the FFT can be accommodated on an XC2V3000 at a sample rate in excess of 200MSPS, with up to a 16K point FFT accommodated on an XC2V6000 without the use of external memory [19]. The initial FFT is followed, for each channel, with one complex multiply per tap for baseband filtering and an inverse FFT, again requiring $MLog_xM$ operations, with M typically being a much smaller number than N. Note that an I/Q balancing block can be inserted immediately following the initial FFT providing for easier support of Zero IF conversion techniques.

Unlike the DDC implementation, where the carrier signal used for mixing is synthesized very accurately, the mixing function of this technique is solely dependent upon the spacing of the FFT bins. As a result, a secondary mixing function may need to be applied after the inverse FFT to fully baseband the channel of interest. In addition, since this mixing operation is performed on a block of data vs. continuous time processing, the effective "carrier phase" of the mixing signal is reset to zero for each block of data, creating a rotating phase offset between each block if the carrier cycle at the A/D sample rate is not an integer multiple of the block size. To compensate for this, a phase rotation would be applied to each output sample, with a different rotation required for each inverse FFT. It should be noted that, in any coherent modulation scheme, some level of frequency and phase adjustment is required after the channelizer anyway, to maintain coherent operation. The carrier compensation requirements for this scheme can therefore be conveniently rolled into this second phase of "tuning", minimizing the computational expense of this part of the channelization algorithm.

Using the FDF channelization approach, a large number of both wideband and narrowband operations can coexist in the same channelizer structure, providing for

improved flexibility and higher channel density than the DDC technique. However to make optimal use of this capability, a programmable device such as a DSP must be used for the baseband channelization processing to support dynamic loading of baseband filtering and inverse FFT components of various sizes on a per channel basis.

4.3. Polyphase FFT Filter Bank

The Polyphase FFT Filter Bank (PFFB) channelizer improves upon the efficiency of the frequency domain filtering technique by assuming redundancy within the frequency plan of the wideband channel [20]. This structure makes use of a polyphase filter to isolate and decimate the various channels, and then employs an FFT to efficiently convert each channel to baseband (see Figure 9). The polyphase filter is created through the decomposition of the low pass filter used to provide channel isolation on a per channel basis. In general, the number of channels in this technique must equal the decimation rate, and as such the sampling rate must be a power of two times the baseband bandwidth.

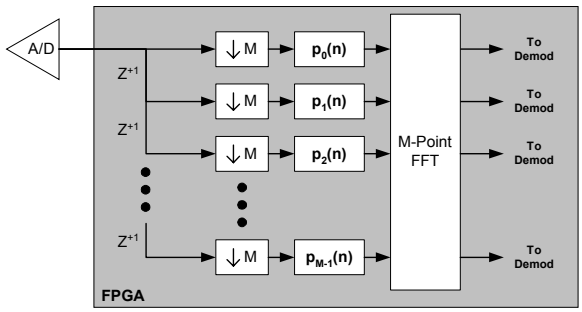

Figure 9: Polyphase FFT Filter Bank Channelizer

Although this technique is limited to channel structures consisting of equally spaced channels, it is extremely efficient, requiring only a single FIR filtering structure and a small FFT, with the FFT typically driving the complexity of the overall channelizer [21]. The entire structure for the channelizer supporting hundreds of channels could be implemented in a single FPGA, with a 64 channel architecture easily fitting on less than half a million gates operating a input speeds of well over 200 MSPS [22, 23]. Other techniques are available to reduce the complexity of this algorithm even further, depending on the specific frequency allocation in use [24].

5. SUMMARY COMPARISON OF CHANNELIZATION TECHNIQUES

A top level functional review of the three channelization techniques presented shows that, although the Polyphase FFT Filter Bank is fairly limited in the types of frequency plans that it can support, the DDC and FDF approaches offer very similar capabilities in terms of flexibility. This comparison extends to performance as well, as evidenced through the simulation of a communications channel supported by each channelizer approach in the presence of additive white gaussian noise. A test bed for such a simulation using a BPSK modulation scheme was developed in Matlab® and is presented in Figure 10.

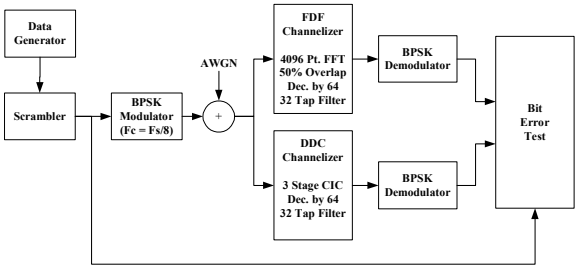

Figure 10: Test Bed for Simulation of Bit Error Rate Performance

The results of the Matlab simulation are presented in Figure 11. The DDC and FDF channelizer schemes tracked fairly well in bit error rate performance, operating to within a dB of theory over the range of signal to noise ratios that were tested. Note that carrier and phase detection where not included in this simulation since they would not materially impact the results. Also, a carrier frequency of Fs/8 was selected for the BPSK waveform to eliminate the need for the frequency and phase offset correction outside of the channelization function.

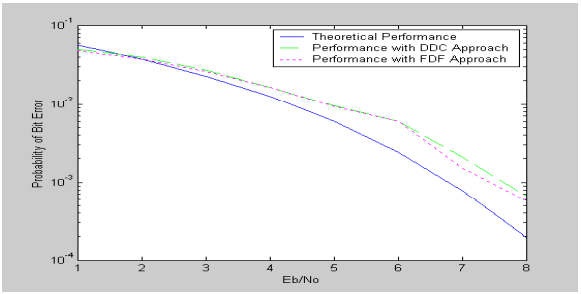

Figure 11: Test Results from Bit Error Rate Simulation

Further comparison between the various channelization approaches is seen by mapping the number of operations per baseband sample against the total number of supported channels, as shown in Figure 12. For this analysis, a decimation of 64 was assumed, and a Radix 4 FFT was utilized for both the FDF and PFFB approaches. As can be seen, for equi-spaced channels, the efficiency of the PFFB approach exceeds the efficiency of the DDC approach after around 3 channels. Similarly, the efficiency of the FDF approach exceeds the DDC for any type of channel spacing and bandwidth after around 18 channels. Even greater computational efficiency can be

obtained if it is possible to move to a higher radix FFT operation.

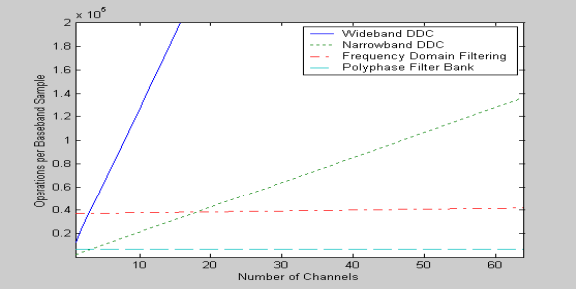

Figure 12: Computational Complexity of Channelization Approaches vs. Number of Channels Implemented

6. CONCLUSIONS

This paper has explored three channelization approaches: the DDC approach, the FDF approach, and the PFFB approach. The analysis shows that bit error rate performance is not a driver in the selection of the channelization architecture. A comparison based on computational complexity, however, reveals that the use of the DDC technique is inefficient beyond a handful of channels. If redundancy exists in the channel structure, then the polyphase FFT filter bank appears to be the most efficient choice, and if flexibility is required, then the FDF approach seems to make the most sense.

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The Matlab simulations presented this paper can be found at:
http://www.spectrumsignal.com/channel_techniques/