# DEVELOPMENT PLATFORM DESIGNED TO SPEED MARKET APPLICATION DESIGNS

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## ABSTRACT

It is expected that in the near future all radio devices will be radio application software executing on reprogrammable hardware thru middleware software the same way that all office automation devices of the 80s have been replaced by office automation application software executing on PC thru operating system. This paper describe a software radio testbed and radio development environment targeted at education and research organization to help them transition to the software radio technology. The radio development environment consists of lab instrumentation, hardware platform, and software tools. An overview of the hardware platform and software tools are described in the paper. A typical radio development process for this new approach is also described to help the reader understand how the tools are being used.

## 1. INTRODUCTION

Today's radios consist of hardware and software solutions. However the hardware is unique for each radio device. It is expected that in the near future all radios will used the same generic reprogrammable hardware platform for all radio, radio application software and middleware software. The middleware software allows the application software to be independent from the hardware solution. In this approach all radio devices consist only of application software. The application software modules use the middleware software to control the behavior of the hardware in order to provide the desired radio functionalities. To develop a radio, a telecommunication engineer first develop the mathematical equation that describes the desired radio behavior. Automatic code generation tools are then used to develop a rapid prototype of the radio that is loaded in the testbed and used in real-life environment. Once the model has been validated, optimized application software modules are developed to increase system performance. All signal generation and processing (e.g. multiple-access, power control, coding, IF filtering) are completely software defined. Like PC hardware and OS, the software radio testbed supports multi-tasking allowing multiple radio devices to operate simultaneously.

## 2. MOTIVATION

The objectives of our a real-time software' radio testbed is to allow research and development (R&D) organizations including universities to use this newer approach for radio development. The software radio testbed allows R&D organization to benefit of the flexibility and speed of a software development environment/tools for advanced mobile communications radio system prototyping for all layers of the protocol stack. The platform helps these organizations transition from a hardware-based radio solution to software-based radio solution. The platform is based on US DoD Software Communication Architecture (SCA) standard . The objective of this standard is to ensure that software solutions are independent from hardware vendor. Radio software applications developed on the platform promotes both industrial and academic collaboration and partnership because the software applications is hardware independent.

The platform's frequency bands, bandwidth, transmit power, receiver sensitivity and multiple users capability meet the requirements of the evolving wireless cellular system radio standards (e.g. 1 G, 2G, 3G and 4G). The reprogrammable processors are, however, by no means limited to the restrictions imposed by these standards.

The testbed has been targeted taking into consideration the needs of the stakeholders described below:

a. **Education**. Complement theoretical courses in modern digital communications with a flexible tool that exposes students to implementation issues which surface in real-time signal processing for the classroom. The testbed shall provide students with the global vision of communication systems. It should also open many avenues for student projects both at the undergraduate and graduate levels in advanced radio design techniques. It is very likely that the

result of these projects could be used by the radio industry.

**b. Research**

1) Fundamental Research. Complement fundamental research in communication theory, advanced signal processing algorithms, as well as experiment with new services and their application to real-world problems. Opportunities in research for transmitter and receiver can be found in **Software RADIO A Modern Approach to Radio Engineering** [1].

2) Theoretical Research Vs Experimental Research. Fundamental research in communication theory and its application to real-world problems result in mathematical models. The platform could be used to allow real-time processing of the mathematical models allowing researchers to see their work put into practice and identify potential implementation issues completing the link between theoretical research and experimental research.

3) Wireless cellular system research. Currently lots of research is being done in wireless cellular systems to address a broad spectrum of problems. The platform shall allow exploration of these issues which include:

- Wideband channel estimation and synchronization
- Modem design and interference rejection algorithms and analysis
- Single-user systems (noise rejection, high data rate)
- Multi-user systems (multi-user detection, interference cancellation). Diversity and space-time processing algorithms to increase spectrum efficiency
- Dynamic Resource allocation
- Multiple-Antenna Systems
- Adaptive Array
- Smart antennas and interference rejection
- Multistage Rake Receiver
- Variable rate coding
- Turbo-coding and iterative decoding
- New services (e.g.localization, E-911)
- New standards (e.g. 3G and wireless LAN deployment)
- Many other opportunities

**c. Radio System Acquisition.** Currently to meet your needs in office automation devices you buy a reprogrammable hardware platform called a personnal computer, an operating system, and the required office automation application software. The US DoD envisioned that in the future to meet their wireless communication needs they will purchase reprogrammable hardware components, middleware software, and the required radio application software solutions. As their need evolve they may buy additional radio application software solutions, upgrade the middleware, upgrade the hardware, or a combination of the above. Like the PC world they expect that there will be many vendor sources for each of the radio components: reprogrammable hardware, middleware software, radio application software and hardware upgrade kits. To ensure this vision will become a reality the US DoD has developed an open standard architecture called the Software Communication Architecture (SCA). The software radio testbed shall be compliant with this open standard.

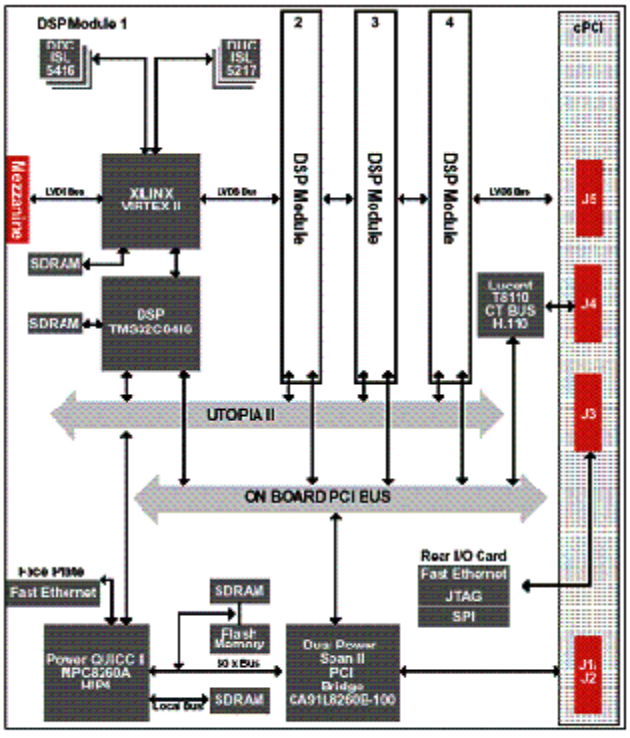


Figure 1: Signal Processing Hardware

## 3. COMPUTATIONAL NEEDS

The ability of a software radio computing platform to implement solutions to the problems identified in the previous paragraph depends on the computational power of the platform. The computational power required for new wireless cellular standards such as UMTS is significantly higher than the first generation standards AMPS. Using the latest DSPs/FPGAs multiple AMPS, GSM/GPRS and EDGE radio sets can be implemented in one of these devices. For CDMAone (IS-95) a combination of FPGA and DSP or DSP and hardware accelerator is required. This combination can handle multiple CDMAone radio sets. FPGA or hardware accelerator is needed because current DSP processors are not fast enough to perform chip rate processing (spreading and despreading). For UMTS multiple FPGAs and DSPs are required to provide the desired computational power. One Commercial-Off-The-Shelf (COTS) solution for UMTS base station requires one FPGA (4 million gates) and three DSPs. Another solution requires three FPGAs (four million gates) and one DSP. As processing power increases researchers are developing new radio solutions that take advantage of the increases in processing power and as a result additional processing power is needed. Multi-User Detection (MUD) and smart antenna technologies are examples of this trend. One COTS MUD algorithm requires the processing power of one FPGA (4 million gates). Even more processing power is required to implement a smart antenna solution.

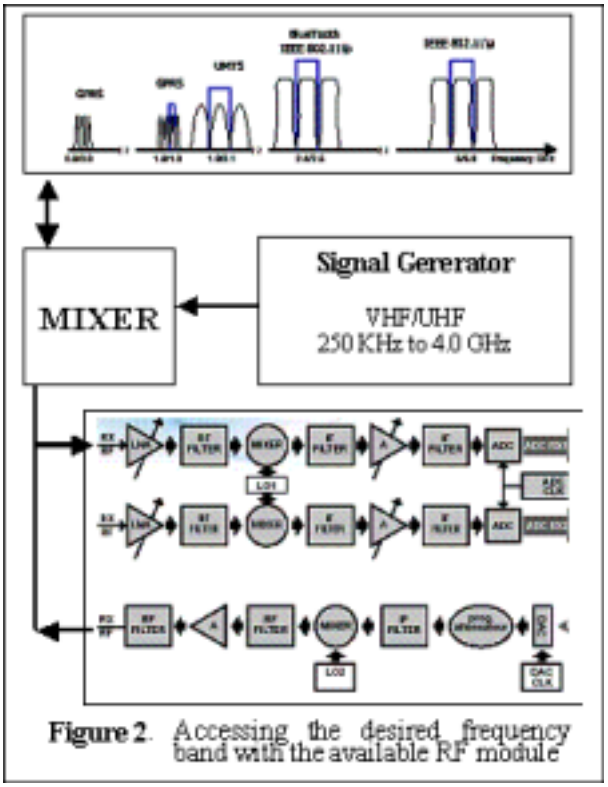


**Figure 2**. Accessing the desired frequency band with the available RF module

## 4. SIGNAL PROCESSING HARDWARE

Following analysis of stakeholder needs it has been determined that the radio computing platform should support the possibility of having up to 16 virtual channels in one processor (DSP or FPGA) as well as supporting the allocation of functionalities for one radio set to 4 FPGAs and 4 DSPs. The signal processing board shown in figure 1 allows the implementation of radio solutions for 3G and beyond wireless cellular system research. This board can provide high computational capability: The main features of the signal processing hardware are:

a. 8 Intersil ISL5416 Quad DDCs and 8 Intersil ISL5217 Quad DUCs. Using one element of the quad the channel bandwidth can be changed in real-time from 1 KHz to 8 MHz. By combining all four elements the channel bandwidth can be changed from 1 KHz to 32 MHz.
b. 4 Xilinx Virtex II FPGA
c. 4 Texas Instruments 600 MHz TMS32C6416 DSP
d. 1 PowerQUICC II MPC 8260A
e. Up to 16 virtual channels in each FPGA and DSP can be selected
f. 6U cPCI

A signal processing board based on PCI mezzanine card has also been developed that provides four times less computational capability. This board has sufficient processing power to teach students development of radio using software radio enabling technology as well as the development of older modems: AM Receiver; Narrowband FM Receiver; Broadcast FM Receiver with stereo recover, FSK data, BPSK, QPSK.

## 5. RF HARDWARE

The software radio testbed also incorporates a programmable RF front-end. Nowadays, the technology does not allow having an ideal software radio receiver that digitized the RF signal at the RF stage (Digital Front-End). The current solution is to use one RF multi-carrier transceiver for each frequency band (standard) being considered. In a RF multi-carrier transceiver using IF sampling, a IF band of up to 35 MHz in bandwidth can be digitised with current Analog-to-Digital Converter (ADC).

The difference between this approach and the one most commonly used is that with multi-carrier transceiver the mixer and IF filter are protocol independent and the digitized IF bandwidth contains the data from all the RF channels present in that bandwidth. With the most common approach the mixers and IF filters are dependent on the modulation and only one RF carrier at IF frequencies is digitised.

Currently a 6U cPCI RF Cellular Module providing a multicarrier, wideband radio front-end that operates in the Rx 824-849/Tx 869-894 band is available for the software radio testbed. The transceiver is independent from the protocol. This provide the flexibility of required to allow the signal processing hardware to support multiple protocol simultaneously.
Currently only one RF multi-carrier card is available. This by no means limits the use of the testbed to the standards operating in this frequency band. Radio applications that operate at other frequency band then the multi-carrier card can be moved to the frequency interval of the available RF cellular module by using the set up shown in figure 2. The RF signal in the frequency range of interest is mixed with the signal from a signal generator to move it to the frequency interval of the available RF cellular module where it is digitised.

The main feature of the mutli-carrier receiver are:

a. Receivers – Analog Section
   - Type. 2 multi-carrier receivers using IF sampling
   - Frequency Range. 824 to 849 MHz
   - Bandwidth. 25 MHz
   - Dynamic Range. 80 dB
   - Sensitivity. –112 dbm
   - RF_Power_Cover_Range. From –112 dbm to –10 dbm

b. Transmitters – Analog Section
   - Type. 1 multi-carrier transmitters using IF sampling
   - Frequency Range. 869 to 894 MHz
   - Bandwidth. 25 MHz
   - Power level. Full Band Maximum 0 dbm
   - Power level. 1 channel Minimum –100 dbm
   - Spurious Free Dynamic Range. 82 dbc
   - Phase Noise Co-channel. –115 dbm/MHz

The multi-carrier transceiver is conceived in order to be configured to handle the following operating modes:

- Real time processing for wideband signals (e.g. UMTS like)
- Real time processing for narrowband signals (e.g. GSM, EDGE)
- Non-real time processing (recording mode for off-line post-processing)
- Direct partial data transfer with non-real time processing

## 6. INTERCONNECTION

A high speed data bus capable of 30 Gbits of data per second that passes the samples directly from the RF modules to the signal processing modules is being developed to allow real-time processing of the samples. With this interconnection, multiple RF cards and multiple signal processing cards can be added allowing the platform to support up to 800 MHz of discontinue RF bandwidth This makes the radio computing architecture both flexible and scalable. This interconnection is based on the requirements defined by OBSAI (Open Base Station Architecture Interface).

## 7. RADIO DEVELOPMENT ENVIRONMENT NEEDED TO SUPPORT THE RADIO DEVELOPMENT PROCESS

The typical radio development process and associated tools are shown in figure 1 and described in the following sub-paragraph. Many tools are needed to support this process. Most of them are already available in R&D laboratories.

**a. System Design.** System Design for radio development consists of system requirements, system architecture definition, allocation of architecture components to processor technologies, behavior modelling and algorithm design and rapid prototyping. These activities and the tools to support them are described in the following paragraphs.

1) **System Requirements & Specifications**. First the researcher/developer has to understand the problem. Many system/software design tools are available to support requirements gathering and analysis. Often a word processing tool is all that is used.
2) **System Architecture.** Next the designer develops a block-level Architecture of the radio system. Many simulation tools such as Matlab Simulink, Elanix System View, Cadence SPW, already offer libraries containing block-level architecture of many radio devices to model the radio behaviour. The decomposition found in these libraries can be used as a starting point for the block-level architecture.
3) **Allocation of blocks/components to processor technologies**. Once the components as well as the interface have been defined, a decision is made on which processor technologies, DSP or FPGA, shall be used to perform the processing. In the past, this decision was solely based on the designer's expertise. However emerging hardware-software co-design tools can be used to help make the decision. Example of such tools include: Cadence SPW, Ptolemy, etc…
4) **Behaviour Modeling and Algorithm Design.** For each block/component behaviour models are developed as well as algorithm using the simulation tools. The simulation tools are used to test the solution.

b. **Rapid Prototyping (Optional).** After the model has been tested many simulation tools allow the generation of DSP-Code (C or C++ code) and FPGA code (VHDL, Verilog, etc) to test the model on the target hardware and in real-world environment. The behaviour model can then be verified in real-time using real life input.

c. **Components design and implementation (Software and Hardware/FPGA)**. For educational purposes as well as fundamental, and experimental research components used for Rapid Prototyping might be acceptable. However for the final solution, the performance of these components is normally not optimal. Therefore, the components must be designed and implemented by taking into consideration the target hardware.

1) **Software**. Some of the software components can be obtained from DSP libraries, others must be developed from scratch. TI offers a DSP support library. Its web site identifies third-party DSP components vendors. Integration of reusable DSP components from libraries with software components developed from scratch, is normally done using TI code composer studio environment. However, other software development tools are compatible with TI DSP.

2) **Hardware/FPGA.** Many vendors offers reusable FPGA components called IP cores. Some of these components are included with Xilinx Foundation development tools. Other can be purchased from Xilinx. Xilinx' web site, like TI, offers many links to third-party companies that offer reusable components. Xilinx has also produced a document that provides guidelines on coding standard that improves reuse. Integration of components from existing libraries or development of components from scratch can be done using many different HDL verification-simulation tools, synthesis tools and integrated development tools from many different vendors including: Model Technology, Cadence, Aldec, Mentor Graphics, Synopsys, Synplicity, Xilinx, etc…

d. **System Integration and Test**. Integration and test of hardware and software components are normally done on the target platform. The tool most commonly used to develop test plans & procedures and record the test results is a word processor. However some companies offer automated tools.

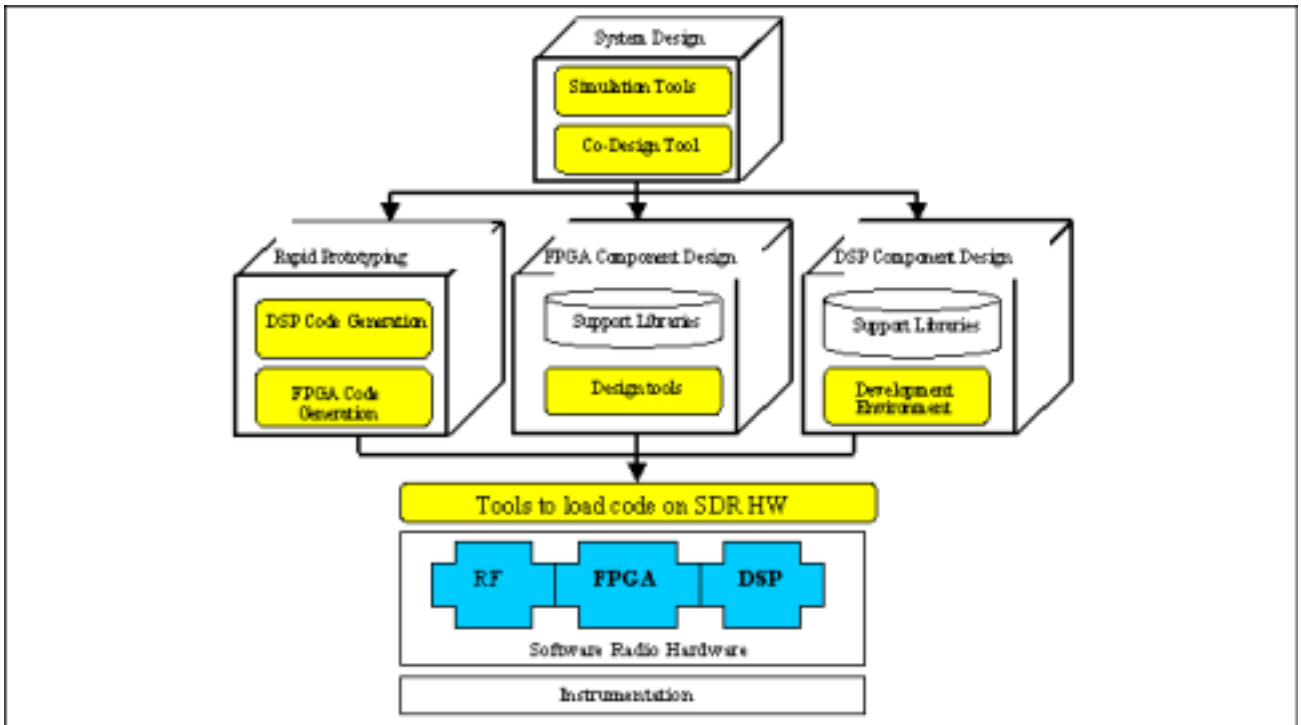


**Figure 3.** Radio development process and tools

## 8. CONCLUSION AND FUTURE WORK

A software radio testbed has been developed that allows the development of radio with unprecedented performance that supports newly proposed signal processing techniques, including: adaptive receiver; adaptive interference suppression, multiuser multistage RAKE receiver, adaptive turbo coding, smart antennas and exploration of many other novel techniques. These innovations can be verified and validated individually or integrated together to evaluate the impact of the different possible combination on the performance of new wireless transceivers. A rapid prototype of the solution can be developed using code generated by the simulation tools and operating on the target hardware. The final solution normally requires code optimized for the targeted processor FPGAs and DSPs. Because the testbed meets the requirements of the SCA, code developed for the platform should be portable on other SCA compliant platform.

In the future we plan on extending our platform to handle multi-antennas. To be able to implement smart antennas technology the software radio testbed shall allow phase synchronization for all mixers and all digitizers (ADC and DAC). Different techniques are possible including the use of a clock generation signal that uses a single source combines with a clock distribution system.

We also intend to develop a component model of a software radio at a lower level of abstraction than the SCA model. This model shall allow rapid component addition or removal and configuration of the software radio components. The focus of this model is to ease adaptability and evolvability of the radio system for future upgrades. Similar work are being done by Networks and Telecommunications Research Group (NTRG) at Trinity College in Dublin Ireland.

Finally the system shall be integrated with Mitsubishi Virtual Field Test Simulator in the near futture. This tool simulate the elctromagnetic environment as well as the behavior of thousands of users bringing near real-life condition in the lab therefore significantly reducing the need for field test trials. The tool allows the development a new protocol and testing of the protocol using almost real condition before its deployment. For example the tool can be used to verify registration and hand-off algorithms in the handset and in the network.

## 10. REFERENCES

[1] Jeffery H. Reed, Software RADIO. A Modern Approach to Radio Engineering, Prentice Hall PTR, New Jersey, 2002.